20MHZ MULTIBUS II PARALLEL SYSTEM BUS INVESTIGATION

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APRIL 8, 1991

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May 10, 1991

The following documents describes in detail the investigation done to date for a 20MHz version of the MBII PSB. It includes all the information used for analysis as well as the changes proposed to arrive at a 20MHz solution.

To complete the investigation and development of a 20MHz specification, the following remains to be done:

1. Read and fully comprehend the contents of this document.
2. Finalize 20MHz MPC timing numbers. This will be done by Intel.
3. Design and prototype the new backplane recommended in this document.
4. Design and prototype the 20MHz CSM module recommended in this document.
5. Build 20 MBII test boards using 20MHz MPC's and using new transceivers.
6. Put together a validation system from the components described above.
   - Use this system to validate some the bus loss timing parameters proposed in this document. Use the results of the validation to trade off various parameters such as bus loss, MPC timing, termination values, etc.
   - Use the system for full functional testing (maybe under environmental extremes).
7. Fully document the results of the above validation in a form acceptable and usable as a new 20MHz PSB Specification.

TABLE OF CONTENTS

INTRODUCTION

The goal of this document is to record the work done to date in arriving at a proposed 20MHz solution for the MBII Parallel System Bus. Several key efforts have supported the belief that such a solution is viable. These are:

- Characterization of Intel's MPC to look at PSB Timing parameters
- A paper study of the timing paths and the constituent elements (MPC, tranceivers, backplane, etc.)
- A simplified backplane lab experiment with new termination values for certain signal groups.

This document also outlines the work that I believe needs to be done before we can call this 20MHz solution "in-the-bag".

The "20MHz Solution" as discussed in this document actually refers to two targeted solutions: a 10-slot system running at 20MHz and a 20-slot system running at 16MHz.

PSB TIMING PATHS & EQUATIONS

The different timing paths that determine the maximum PSB frequency are shown in Figure 1 and the associated timing equations shown in Table 1. Note that the clock-to-data and clock-skew parameters are referenced at the MPC instead of where the board interfaces to the PSB backplane as with the IEEE 1296 specification. This more easily serves the purpose of this analysis. For a strict backplane specification, these parameters can be referenced back to the board-backplane interface at a later time.

The timing equations in Table 1 are reasonably straightforward. However, notice that there is no timing requirement for the low-to-tristate transition for BAD13-BAD0 and BPAR3-BPAR0. This is valid for the two possible situations. Firstly, in the very next cycle following the tristate condition, the next bus agent may immediately drive the BAD and BPAR signals. In this case the signals will arrive at a valid logic level within the setup time of the next clock. Secondly, if another agent does not drive these signals in the next cycle, then the signals will simply float high (but probably not within the next setup time). This situation is acceptable since the bus state machines do not expect these signals to hold valid data during those cycles.

MPC NUMBERS

Table 2 shows a summary of the test data from the characterization of Intel's MPC. Table 3 is a strawman specification for a 20MHz MPC based on the results of the characterization. Note that the timing parameters are specified slightly differently than the old MPC spec. For example, the Tcd parameter is separated into two: one for the high-to-low transition and one for the low-to-high. In addition, the setup times and the arbitration logic loop delay parameters are specified by design in the strawman.

TRANSCEIVERS

After looking at several transceiver options, the Signetics ABT BiCMOS '245 was chosen. It has low propagation delay times and low output capacitance (7pF). The spec is shown in Appendix A. At the time of writing, similar devices are being introduced or developed by TI and National. Also considered were the new National FASTr family of logic devices and the TI BCT25645 25-ohm transceiver. While the FASTr family had smaller prop delays than the ABT family, it was unsuitable because of high output capacitance (18pf). The BCT25645 was not chosen because of its incompatible pinout and the "Wired-Or" glitch problem.

Of some concern with the transceivers is the simultaneous switching output (SSO) effect. This occurs when all outputs of a particular device transition in the same direction (HL or LH) at the same time. This degrades the Tpd's of the device. Interestingly enough, this effect was not documented with earlier logic families (the Tpd figures were only for a single output switching). The derating curve shown in the ABT

specification is for all packages - including the DIP package. On contacting Signetics, characterization data was obtained for an ABT244 that shows the difference in this SSO degradation between an SOIC and a DIP package (Appendix B). Note that the SSO effect for the SOIC part is less. This issue should be further investigated.

BACKPLANE CHARACTERIZATION

Investigation Methodology

The IEEE1296 backplane specifications were derived from extensive analysis and measurements and have been proven reliable over years of use. With this new 20MHz version of the MBII PSB, three methods can be used to specify backplane timing parameter values. The first is a paper analysis using theoretical equations for backplane behavior to derive backplane timing numbers. The second is Spice simulation of the backplane environment. Lastly, a full lab measurement can be done.

The approach taken in this document is to combine a paper analysis with a lab measurement for validation. Since the hardware needed to do the lab measurements is relatively easily available, I do not feel that the Spice simulation is worth the effort. The paper analysis is detailed later in this document. While a simplified lab experiment was done to validate some of the analysis, a more thorough and detailed lab measurement remains to be done.

Parameters of Interest

According to Table 1, there are 15 separately defined bus loss parameters for the six different timing paths:

Timing Parameters	Backplane tranceivers
TbusHL1, TbusHL2, TbusZL1	ABT245
TbusHL2, TbusLH2, TbusZL2, TbusLZ2	ABT245
(TbusHL3, TbusLH3	F245)
TbusZL4, TbusLZ4	Direct from MPC
TbusHL5, TbusLH5	ABT245
TbusZL6, TbusLZ6.	Direct from MPC

The timing parameters denoted with HL refer to the case where a signal is driven from an high level to a low level. LH refers to the opposite. ZL refers to the case where a signal is driven from tri-state to a low level and LZ refers to a signal being tristated by a tranceiver and being pulled high by the backplane terminations.

The 15 parameters can be further classified by the type of backplane tranceiver in order to ease the analysis:

Timing Parameters	Backplane tranceivers
TbusHL, TbusLH, TbusZL, TbusLZ	ABT245
TbusZL, TbusLZ	Direct from MPC

For the most part, the old PSB spec treated the high-to-low and low-to-high transitions as a single timing equation. For this analysis, the two are separated as shown in Table 1. This allows the high-to-low timing equation to take advantage of the fact that the high-to-low transitions on the backplane (TbusHL and TbusZL) only require one bus delay.

Transmission Line Paper Analysis

Before numbers can be assigned to the backplane timing parameters outlined above, it is necessary to derive several key backplane characteristics. This analysis is shown in Table 4. The important results from Table 4 are the effective impedance and the different bus delays.

The parameter TbusLZ described in the previous section is of particular interest. The IEEE1296 spec allowed three bus delays from when the driver began to turn off to when the signal returned to a high

logic level. This amounted to 34ns. To achieve 20MHz operation, this parameter has to be reduced to two bus delays. This requires the use of new termination values that increase the amount of the low level output current (IOL) and is discussed in the following section. Note that this requirement does not apply to the BAD and BPAR signals for reasons described above.

With the IEEE1296, TbusHL and TbusZL were specified as taking a one way delay while TbusLH was specified as a round trip delay. These are assumed to be the same for this 20MHz spec.

To simplify the timing analysis, the results from Table 4 are aggregated for either type of transceiver (ABT245 or MPC-direct). Taking all the above into consideration, the following numbers are assigned to the various backplane timing parameters:

20 Slots:	One Way Delay	TbusHL, TbusZL	15ns
	Round Trip Delay	TbusLH, TbusLZ	25ns
10 Slots:	One Way Delay	TbusHL, TbusZL	10ns
	Round Trip Delay	TbusLH, TbusLZ	15ns

In summarizing this section, realize that the timing numbers derived are based on simplified backplane equations that may not take into account various second order backplane effects. Therefore, they should be used with caution. To be more accurate, a real backplane measurement should be done; the results of a simplified lab measurement is described later in this document.

New Termination Requirements

As mentioned above, new terminations are required for the SCx, BREQ, RSTNC, BUSERR and ARBx signals so that TbusLZ only uses a round trip backplane delay. The proposed new termination values are 130 ohms over 220 ohms. This increased the amount of output current that the bus driver has to sink (IOL) and increases the incident current step which occurs when the driver turns off. This leads to a bigger voltage step after turn-off and a valid high voltage level (VOH) is achieved after the voltage step has propagated to the other end of the backplane and back.

To aid in the analysis, a Bergeron diagram is employed (Appendix C). From this, equations are derived that predict the voltage level after the round trip delay (V2). These equations are used in Table 5 to also calculate the amount of current that the driver has to sink. The total output current (IOL) is the sum of that sourced by both terminations and the total of all other tristated bus drivers (Iil +Iozl).

From Table 5, the second voltage step (V2) is calculated to be 2.41V and 2.28V for the ABT transceivers and the MPC-drivers respectively. The MPC-driver's second voltage step is lower mainly due to the larger output capacitance and lower effective backplane impedance.

The maximum output current calculated from Table 5 is close to the maximum limit of 64mA for the ABT transceivers. Different termination values should be considered if it is felt that there is insufficient margin. The trade-off will be between reducing the output current and reducing the second voltage step. This decision should be made after lab measurements that more accurately determine the second voltage step value.

The maximum output current also exceeds the old MPC spec of 60mA. However, the characterization results indicate that this spec may be increased to 70mA (extrapolated from the characterization data in Table 3 which shows IOL of 80mA at 0.61V).

Preliminary Measurements

A simplified lab experiment was done to get an early verification of the results of the paper analyses above. This experiment was simple in that passive capacitors were used for the backplane load instead of real transceivers; however, the actual bus transceivers were used to drive the backplane. The experiment

was done with a 20-slot backplane at room temperature and 4.75 supply voltage. The system was only operated to be able to get signal scope measurements. No exhaustive functional backplane tests were done.

The experiment results include the National FASTr version of the '245 transceiver that was also being evaluated at the time.

The experiment concentrated on the backplane operations which were different from the IEEE1296 spec - namely, the termination change and round trip operation of MPC-direct signals and the SCx signals.

The experiment and its results are included in Appendix D. The results of the experiment are summarized as follows:

	TbusLZ	V2	TbusZL
ABT245	18ns	2.6V	9ns
FR245	22ns	2.3V	12ns
MPC-direct	22ns	2.2V	10ns

Note that the results are better than that derived in the preceding paper analyses. However, due to the simplified nature of the experiment, it should be recognized that there is still room for error. A more thorough lab measurement/backplane characterization is required.

Finally, note that on the high-to-low transition (TbusZL or TbusHL) of all signals, there is significant positive reflection up to 1V in magnitude. If this is found to persist when a more thorough experiment is done, then diode clamps at the signal terminations should be considered to minimize this reflection.

CLOCK SKEW

The clock skew discussed in this document refers to the skew between the rising clock edges at the clock input to every MPC in the system. As such, it includes mainly two components of skew: the backplane skew and the skew due to different prop delays of the local buffer/inverter (usually a AS1004). The IEEE1296 allowd for 5ns of backplane skew and achieved this using a bussed clock driven from the center of a 20-slot backplane. The local buffer was allocated 4.5ns of skew. However, 1.5ns of this was due to possible input level shift which was exarcebated by the bussed clock signal and its slower edge rates.

In order to achieve 20MHz operation it will be seen later that a total clock skew of about 4ns is required. The solution proposed here is to implement a radially-distributed clock system using a clock-driver resident on the backplane itself. This should decrease the backplane skew to about 1ns.

Proposed CSM-002 Solution

Such a solution is illustrated in Figure 2 for MBII boards supplying CSM functionality via a CSM-002 module. Appendix E includes the data sheet for one possible clock driver device with 700ps output-to-output skew. To arrive at the desired 1ns, only 300ps are left for trace-to-trace skew. With careful layout and trace length matching, this should be possible. Of course, this should be verified by actual characterization/measurement. For the solution proposed, each clock driver output drives at most two board inputs. This should yield steeper clock edges at the local buffer input compared to the bussed clock solution and eliminate the level shifting phenomena and reduce the local buffer skew to 3ns.

NEW TIMING NUMBERS

Tables 6A and 6B detail the timing equations using the timing numbers derived above for the various delay elements. These two tables match exactly with Table 1 and done for both a 20-slot and a 10-slot backplane. Based on this preliminary analysis, the results show that a 20-slot/16MHz and a 10-slot/20MHz solution are within range.

COMPATIBILITY IMPLICATIONS

The key philosophy in the decisions for this 20MHz solution were to maintain as much as possible the existing hardware investments made by MMG members. However, nothing is free and the following itemizes the new hardware investments needed:

1. 20MHz MPC to replace old MPC
2. New Backplane and terminations
3. New 20MHz CSM solution
4. New transceiver

CSM Compatibility Issues

If a fixed frequency CSM solution is employed, then old 10MHz boards will obviously not work in a 16MHz or 20MHz system (however, new boards will function in an old 10MHz backplane). A more elaborate CSM solution would be to allow frequency selection at power-on. The CSM could be configured to 10MHz if 10MHz-boards are present in the backplane, i.e. the new backplane/CSM would easily support both old and new boards.

At the time of writing, Signetics is not planning to offer the '242 Quad Bus transceiver as part of its ABT family. This device is currently used as the TIMOUT signal bus transceiver on existing MBII boards that support the CSM-002 module. Unless Signetics or some other vendor adds the '242 to their ABT family, old CSM-002 capable boards cannot be easily upgraded to the 20MHz spec. New boards being designed to support the CSM-002 should use the ABT245 in place of the '242. Non-CSM-002 capable boards typically use a AS1004 to buffer the TIMOUT signal and are not affected by the lack of a ABT242.

DIP vs. SOIC

As mentioned in the transceiver section above, the simultaneous switching output (SSO) degradation is worse for DIP packages compared to SOIC packages. Further investigation should be done in order to determine if this 20MHz solution will function with DIP transceiver packages. The worse outcome of the results would be that only SOIC packages are allowable for the bus transceivers.

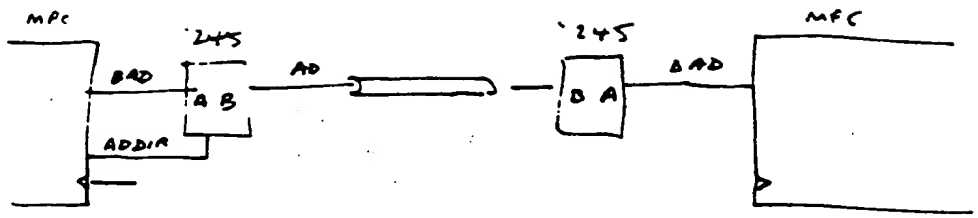
REMAINING WORK

Before the 20MHz PSB specification can be completed, the following still remains to be done:

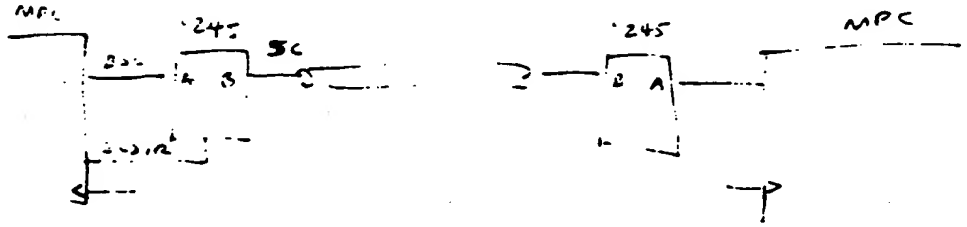
- Design and prototype of a new backplane to support a radially distributed clock including the new termination requirements.
- Design and prototype of a 20MHz CSM module or board.
- A complete backplane lab experiment with new transceivers for full characterization and validation of the bus loss timing parameters and signal quality. Ideally, should be done for both 10-slot and a 20-slot backplane.
- A system validation effort where a fully populated system is functionally tested (maybe under environmental extremes).
- Resolving miscellaneous issues such as ABT242 availability for CSM-002 support, Simultaneous Switching Output effect of ABT245 tranceivers, etc.

FIGURE 1

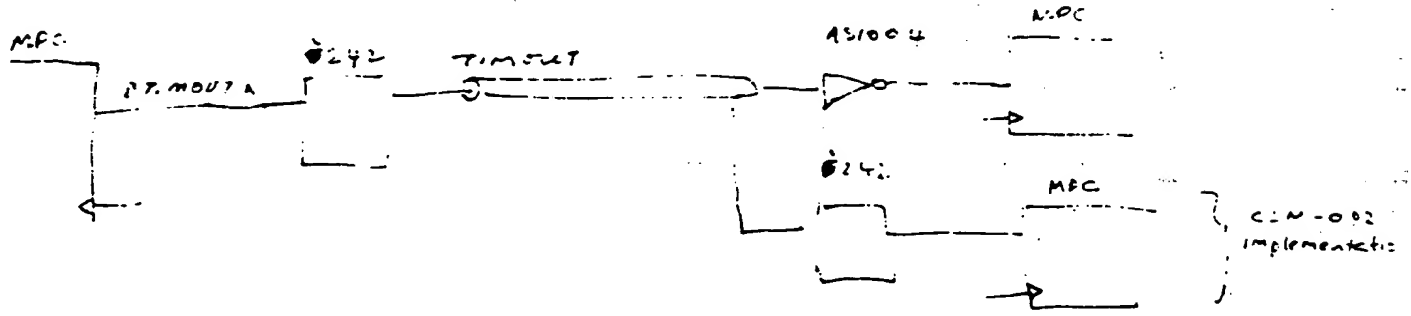
AD, PAR



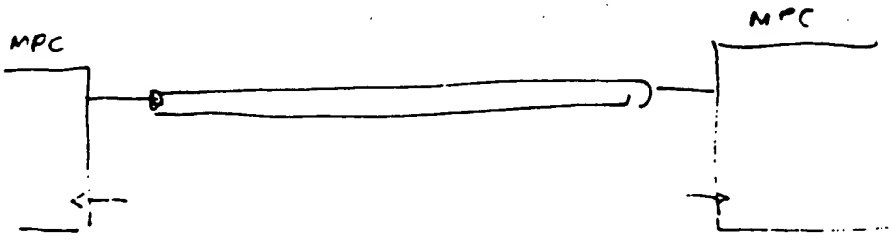
SC



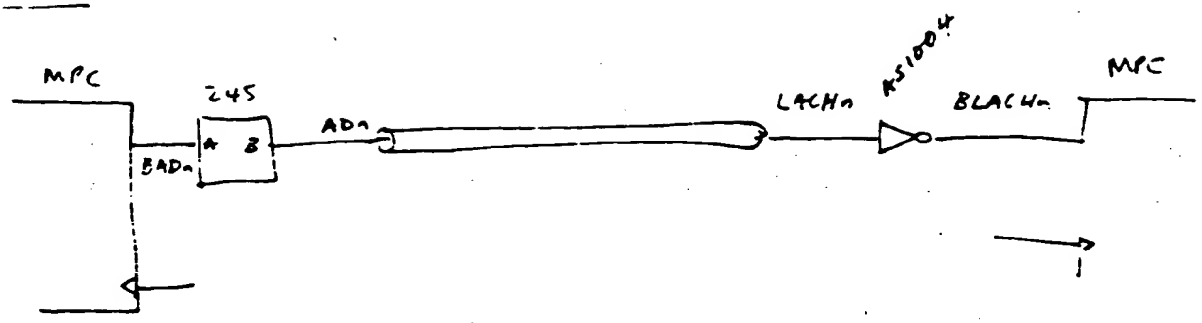
T. MOUT



BREQ, RSTNC, BUSERR



LACHn



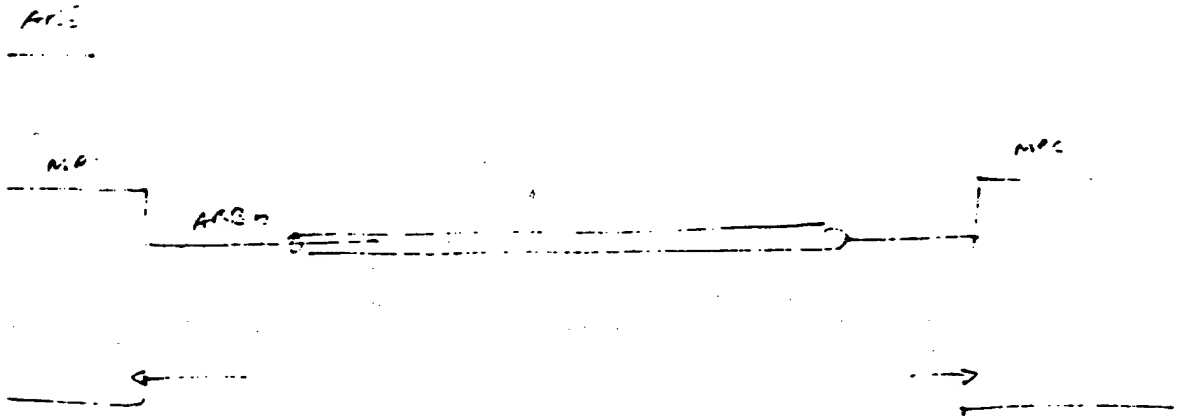
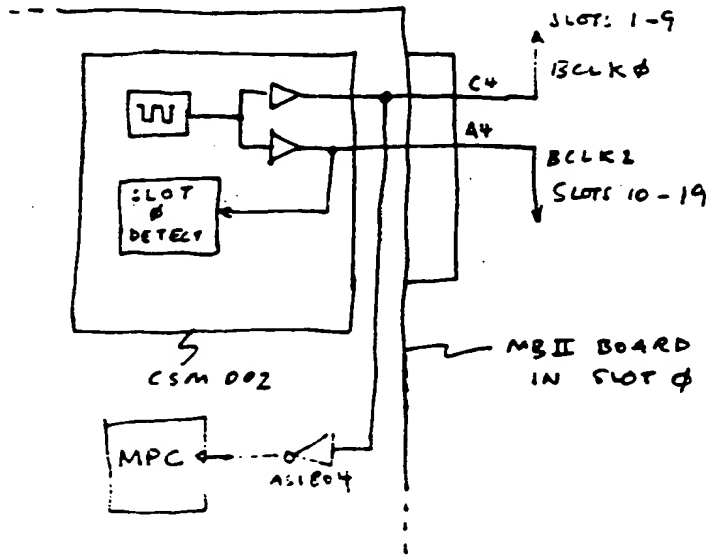


FIGURE 2

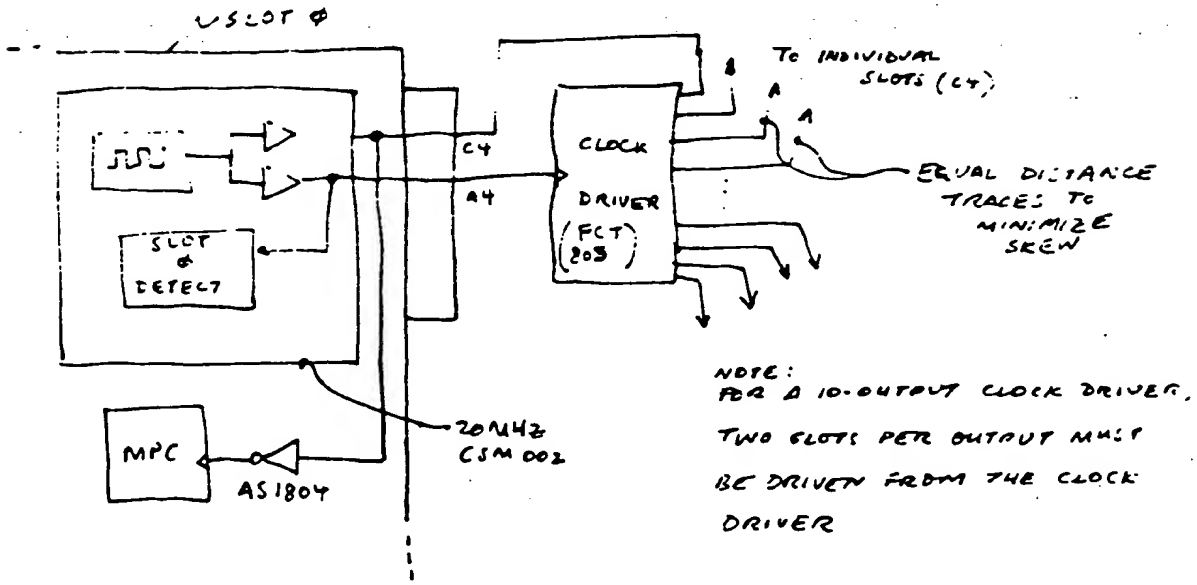
20MHz PSB CLOCK DISTRIBUTION SOLUTION

T. MA, INTEL CORP.
1/24/96

CURRENT CSM 002 SOLUTION:



20MHz PSB, RADIALLY DISTRIBUTED CLOCK SOLUTION:



- STILL NEED TO LOOK CCLK AND TIMING.
- SHOULD CLOCK LINES BE SERIES TERMINATED?

TIMING REQUIREMENTS FOR MAXIMUM CLOCK PERIOD

BAD31-BAD0, BPAR3-BPAR0

		MPC Clk-to-data		ABT245		BUS LOSS		ABT245		MPC Setup		Clk skew
High to Low	Total =	T1	+	TPHL	+	TbusHL1	+	TPHL	+	T23	+	Tskew
Low to High	Total =	T9	+	TPLH	+	TbusLH1	+	TPLH	+	T23	+	Tskew
Tristate to Low	Total =	T10	+	TPZL	+	TbusZL1	+	TPHL	+	T23	+	Tskew

BSC9-BSC0

		MPC		ABT245		BUS LOSS		ABT245		MPC		Clk skew
High to Low	Total =	T1	+	TPHL	+	TbusHL2	+	TPHL	+	T23	+	Tskew
Low to High	Total =	T9	+	TPLH	+	TbusLH2	+	TPLH	+	T23	+	Tskew
Tristate to Low	Total =	T11	+	TPZL	+	TbusZL2	+	TPHL	+	T23	+	Tskew
Low to Tristate	Total =	T5	+	TPLZ	+	TbusLZ2	+	TPLH	+	T23	+	Tskew

TIMOUT

		MPC		F242		BUS LOSS		F242		MPC		Clk Skew
High to Low	Total =	T6	+	TPHL	+	TbusHL3	+	TPHL	+	T23	+	Tskew
Low to High	Total =	T12	+	TPLH	+	TbusLH3	+	TPLH	+	T23	+	Tskew

BREQ, RSTNC, BUSERR

		MPC			BUS LOSS			MPC		Clk skew
Tristate to Low	Total =	T2	+		TbusZL4	+		T25	+	Tskew
Low to Tristate	Total =	T19	+		TbusLZ4	+		T25	+	Tskew

LACHn

		MPC		ABT245		BUS LOSS		AS1004		MPC		Clk Skew
High to Low	Total =	T1	+	TPHL	+	TbusHL5	+	TPHL	+	T23	+	Tskew
Low to High	Total =	T9	+	TPLH	+	TbusLH5	+	TPLH	+	T23	+	Tskew

ARBITRATION SEQUENCE (over 3-clock cycles)

	MPC Clk-to-data		MPC Logic loop		BUS LOSS		BUS LOSS		MPC Setup		Clk Skew
Total =	(T20 \ T3)	+	3* T33	+	2*TbusZL6	+	2*TbusLZ6	+	T26	+	Tskew

With values of the T's

TIMING REQUIREMENTS FOR INPUT HOLD TIME

BAD31-BAD0, BPAR3-BPAR0

	MPC Output Hold		ABT245		ABT245		Clk skew
Output Hold Available =	T17	+	TPD(min)	+	TPD(min)	-	Tskew
Input Hold Requirement =	T27						

BSC9-BSC0

	MPC Output Hold		ABT245		ABT245		Clk skew
Output Hold Available =	T18	+	TPD(min)	+	TPD(min)	-	Tskew
Input Hold Requirement =	T28						

BREQ, RSTNC, BUSERR

	MPC Output Hold		Clk skew
Output Hold Available =	T15	-	Tskew
Input Hold Requirement =	T31		

ARB5-ARB0

	MPC Output Hold		Clk skew
Output Hold Available =	T16	-	Tskew
Input Hold Requirement =	T32		

TABLE 2
MPC Test Summary Data
Taufik Ma **2/7/91**
Slow numbers are the worse figures from 4 parts (two SS, two SF) at 85 degrees and 4.75V.
Typical numbers are from one part under the same conditions.
Tester Load Capacitance used is about 45pF.

		Fast	Typ	Slow		
TCP	Clock Period					
TBCL	BCLK Low Time					
TBCH	BCLK High Time					
TR	BCLK Rise Time					
TF	BCLK Fall Time					
TCD,HL	Clock to HL output delay					
	BAD31-BAD0		13.6	14.7		
	BPAR0-BPAR3		11.0	12.2		
	BSC0-BSC9		11.3	12.4		
	TIMEOUT		10.6	11.3		
	BREQ		12.0	13.2		
	RSTNC		11.7	12.6		
	BUSERR		12.1	13.0		
	ARB0-ARB5		13.0	14.0		
TCD,LH	Clock to LH output delay					
	BAD31-BAD0		10.2	11.2		
	BPAR0-BPAR3		9.6	10.6		
	BSC0-BSC9		9.4	10.4		
	TIMEOUT		9.4	10.2		
TOFF	Turn-off delay from clock					
	BREQ		11.0	11.8		
	RSTNC		11.1	11.9		
	BUSERR		13.3	11.2		
	ARB0-ARB5		11.1	12.2		
TCD,HL	Clock to HL output delay					
	ADDIR		8.0	9.0		
	SCDIR0-SCDIR1		8.6	9.6		
TCD,LH	Clock to LH output delay					
	ADDIR		7.4	8.2		
	SCDIR0-SCDIR1		8.1	8.9		

		Min	Max	Units	Conditions
VOL2	Low output voltage at 80mA for Open Collector signals		0.61	Volts	across all 5 parts at 85C
CIO	I/O Capacitance for open collector signals[1]	10.0	11.6	pF	15mV, 1MHz

[1] Capacitance measurements were done on a single typical part.

Preliminary Specifications for 20MHz MPC, 5V+/- 5%, TA=0 to 70 degrees C.
Taufik Ma 4/8/91
(refer to current Intel Data sheet for a more detailed description of Timing Parameters, all unspecified timing parameters are TBD)

		Min(ns)	Max(ns)	Name	Test Conditions
TCP	Clock Period	49.9			
TBCL	BCLK Low Time	20			
TBCH	BCLK High Time	20			
TR	BCLK Rise Time	0.5	1		
TF	BCLK Fall Time	0.5	1		
TSK	BCLKn to BBCLK Skew				
TCD,HL	Clock to HL output delay				
	BAD31-BAD0, BPAR0-BPAR3,				
	BSC0-BSC9		15	T1	CL = 50pF
	BREQ, RSTNC, BUSERR		14	T2	(Note 2)
	ARB0-ARB5		14	T3	(Note 2, 3)
	ADDIR		9	T4	CL = 50pF
	SCDIR0-SCDIR1		10	T5	CL = 25pF
	TIMOUT		12	T6	CL = 25pF
	REFADR		12	T7	CL = 75pF
	SEL		12	T8	CL = 50pF
TCD,LH	Clock to LH output delay				
	BAD31-BAD0, BPAR0-BPAR3,				
	BSC0-BSC9		12	T9	CL = 50pF
	ADDIR		9	T10	CL = 50pF
	SCDIR0-SCDIR1		9	T11	CL = 25pF
	TIMOUT		11	T12	CL = 25pF
	REFADR		12	T13	CL = 75pF
	SEL		12	T14	CL = 50pF
TON	Turn on delay from clock				
	(same as 10MHz part)				
	BREQ, BUSERR, RSTNC	6.5		T15	
	ARB0-ARB5	6.5		T16	
	BAD0-BAD31, BPAR0-BPAR3	5		T17	
	BSC0-BSC9	4		T18	
TOFF	Turn-off delay from clock				
	BREQ, RSTNC, BUSERR		12	T19	
	ARB0-ARB5 (note 3)		13	T20	
	BAD31-BAD0, BPAR0-BPAR3,		15	T21	
	BSC0-BSC9, TIMEOUT		15	T22	
TSU	Input setup time to clock				
	BAD0-BAD31, BPAR0-BPAR3,				
	BSC0-BSC9,				
	TIMEOUT, LACHn, RESET	12		T23	
	COM, ERR	20		T24	
	BREQ, BUSERR, RSTNC	15		T25	
	ARB0-ARB5 (note 3)	20		T26	
TIH	Input Hold Time from clock (same as 10MHz Spec)				
	BAD0-BAD31, BPAR0-BPAR3,	3		T27	
	BSC0-BSC9,	2		T28	

TABLE 3

	TIMEOUT, LACHn, RESET	2		T29	
	COM, ERR	3		T30	
	BREQ, BUSERR, RSTNC	0		T31	
	ARB0-ARB5	0		T32	
TH	Hold Time from Clock (same as 10MHz spec)				
	BREQ, BUSERR, RSTNC	6.5			
	ARB0-ARB5	6.5			
	BAD0-BAD31, BPAR0-BPAR3,	5			
	BSC0-BSC9,	4			
	SCDIR0, SCDIR1	4			
	ADDIR	5			
	REFADR	4			
	SEL	4			
TLOGIC	Arbitration logic loop delay		20	T33	
IOL1	Open Collector Output Low Current	70mA			VOL = 0.55V

TRANSMISSION LINE ANALYSIS
Taufik Ma, Intel Corporation, April 5, 1991

TRACE (STUB) CHARS:		Prop delay (ns/ft)	1.75 (microstrip)
Impedance (ohms)	80	Trace Length (in)	2.5 (same as IEEE1296)
Trace Inductance (nH)	29.17	Trace Cap. (pF)	4.56
Package Induc.	10.00		
Connector Induc.	15.00		
TOTAL INDUCTANCE	54.17		

BACKPLANE:		ABT245	MPC	NOTES
Intrinsic Impedance	Z0(ohms)	72.50	72.50	(IEEE1296 specs 65-80 ohms)
Intrinsic Prop Delay	T0(ns/ft)	2.20	2.20	(stripline)
Signal Inductance	Lsig(nH)	54.17	54.17	
Capacitance(pF)				
Trace		4.56	4.56	
Connector		2.00	2.00	
Device		7.00	13.00	
TOTAL	Cd(pF/slot)	13.56	19.56	
Maximum spec'd	Cd(pF/slot)	15.00	20.00	(IEEE1296 specs 20pF max)
BACKPLANE CHARACTERISTICS				
Effective Impedance	Zeff(ohms)	24.99	21.97	
Prop Delay/slot	Tbp(ns/slot)	0.43	0.48	
Rise/Fall Time	Tr/f (ns)	4.98	5.67	
TIMING ANALYSIS				
20 SLOTS:				
Round trip delay	Tbus (ns)	22.00	25.03	
One Way Delay	Tbus (ns)	13.49	15.35	
10 SLOTS:				
Round trip delay	Tbus (ns)	13.49	15.35	
One Way Delay	Tbus (ns)	9.24	10.51	

Effect of distributed capacitance on backplane impedance:

$$Zeff = \frac{Z0}{\text{sqrt}(1 + Cd * Z0 / T0)}$$

Effect of distributed capacitance on backplane propagation delay:
Tbp = T0 * sqrt(1 + Cd * Z0 / T0)

Effect of signal inductance on rise/fall time (basically LR time constant):
Tr/f = 2.3 * Lsig / Zeff

Round trip signal timing:
Tbus = 2 * Nslots * Tbp + Tr/f

Bus loss for high-to-low transition on BAD lines (single bus delay):
Tbus = Nslots * Tbp + Tr/f

Note: Correction factors for Cd (pF/slot) and T0 (ns/ft) must be used.

OPEN DRAIN/COLLECTOR SWITCHING VOLTAGE LEVELS

Type of transceiver		IEEE1296	ABT245	MPC-direct
Supply voltage	VCC(V)	5.00	5.00	5.00
Pull-up resistance	RU(ohms)	220.00	130.00	130.00
Pull-down resistance	RD(ohms)	330.00	220.00	220.00
Termination Voltage	VT (V)	3.00	3.14	3.14
EffectiveTermination Res.	RT (ohms)	132.00	81.71	81.71
Effective Impedance	ZO (ohms)	22.00	25.00	22.00
	VOL	0.55	0.55	0.55
	I0	-1.86E-02	-3.17E-02	-3.17E-02
	I1	1.33E-02	1.69E-02	1.83E-02
First Voltage Step	V1	1.25	1.76	1.65
	I2	-9.47E-03	-8.96E-03	-1.05E-02
Second Voltage Step	V2	1.75	2.41	2.28
	I3	6.76E-03	4.76E-03	6.06E-03
Third Voltage Step	V3	2.11	2.75	2.65
Effective output current	IOL (mA)	37.12	63.46	63.46
Max Input Current	Iil+Iozl(mA)	1.00	0.05	0.10
Number of slots	N	20.00	20.00	20.00
Allowance for IIL's	N*IIL (mA)	20.00	1.00	2.00
Max Output current	IOL (mA)	57.12	64.46	65.46

TABLE 6A

TIMING REQUIREMENTS FOR MAXIMUM CLOCK PERIOD (20 slots)

Clk Skew = 4

BAD31-BAD0, BPAR3-BPAR0

		MPC Clk-to-data		ABT245		BUS LOSS		ABT245		MPC Setup		Clk skew			Freq(MHz)
High to Low	Total =	15	+	4.6	+	15	+	4.6	+	12	+	4	=	55.2	18.115942
Low to High	Total =	12	+	4.6	+	25	+	4.6	+	12	+	4	=	62.2	16.0771704
Tristate to Low	Total =	9	+	6.3	+	15	+	4.6	+	12	+	4	=	50.9	19.6463654

BSC9-BSC0

		MPC		ABT245		BUS LOSS		ABT245		MPC		Clk skew			
High to Low	Total =	15	+	4.6	+	15	+	4.6	+	12	+	4	=	55.2	18.115942
Low to High	Total =	12	+	4.6	+	25	+	4.6	+	12	+	4	=	62.2	16.0771704
Tristate to Low	Total =	9	+	6.3	+	15	+	4.6	+	12	+	4	=	50.9	19.6463654
Low to Tristate	Total =	10	+	6.3	+	25	+	4.6	+	12	+	4	=	61.9	16.1550889

TIMOUT

		MPC		ABT245		BUS LOSS		ABT245		MPC		Clk Skew			
High to Low	Total =	12	+	4.6	+	15	+	4.6	+	12	+	4	=	52.2	19.1570881
Low to High	Total =	11	+	4.6	+	25	+	4.6	+	12	+	4	=	61.2	16.3398693

BREQ, RSTNC, BUSERR

		MPC			BUS LOSS			MPC		Clk skew			
Tristate to Low	Total =	14	+		15	+		15	+	4	=	48	20.8333333
Low to Tristate	Total =	12	+		25	+		15	+	4	=	56	17.8571429

LACHn

		MPC		ABT245		BUS LOSS		AS1004		MPC		Clk Skew			
High to Low	Total =	15	+	4.6	+	15	+	4	+	12	+	4	=	54.6	18.3150183
Low to High	Total =	12	+	4.6	+	25	+	4	+	12	+	4	=	61.6	16.2337662

ARBITRATION SEQUENCE (over 3-clock cycles)

		MPC Clk-to-data		MPC Logic loop		BUS LOSS		BUS LOSS		MPC Setup		Clk Skew			
	Total =	13	+	60	+	30	+	50	+	20	+	4	=	178	16.8539326
		14													

TIMING REQUIREMENTS FOR INPUT HOLD TIME

BAD31-BAD0, BPAR3-BPAR0

	MPC Output Hold		ABT245		ABT245		Clk skew		
Output Hold Available =	5	+	1	+	1	-	4	=	3
Input Hold Requirement =	3								

BSC9-BSC0

	MPC Output Hold		ABT245		ABT245		Clk skew		
Output Hold Available =	4	+	1	+	1	-	4	=	2
Input Hold Requirement =	2								

BREQ, RSTNC, BUSERR

	MPC Output Hold		Clk skew		
Output Hold Available =	6.5	-	4	=	2.5
Input Hold Requirement =	0				

ARB5-ARB0

	MPC Output Hold		Clk skew		
Output Hold Available =	6.5	-	4	=	2.5
Input Hold Requirement =	0				

TABLE 6B

TIMING REQUIREMENTS FOR MAXIMUM CLOCK PERIOD (10 slots)

Clk Skew = 4

BAD31-BAD0, BPAR3-BPAR0

		MPC Clk-to-data		ABT245		BUS LOSS		ABT245		MPC Setup		Clk skew			Freq(MHz)
High to Low	Total =	15	+	4.6	+	10	+	4.6	+	12	+	4	=	50.2	19.9203187
Low to High	Total =	12	+	4.6	+	15	+	4.6	+	12	+	4	=	52.2	19.1570881
Tristate to Low	Total =	9	+	6.3	+	10	+	4.6	+	12	+	4	=	45.9	21.7864924

BSC9-BSC0

		MPC		ABT245		BUS LOSS		ABT245		MPC		Clk skew			
High to Low	Total =	15	+	4.6	+	10	+	4.6	+	12	+	4	=	50.2	19.9203187
Low to High	Total =	12	+	4.6	+	15	+	4.6	+	12	+	4	=	52.2	19.1570881
Tristate to Low	Total =	9	+	6.3	+	10	+	4.6	+	12	+	4	=	45.9	21.7864924
Low to Tristate	Total =	10	+	6.3	+	15	+	4.6	+	12	+	4	=	51.9	19.2678227

TIMOUT

		MPC		ABT242		BUS LOSS		ABT242		MPC		Clk Skew			
High to Low	Total =	12	+	4.6	+	10	+	4.6	+	12	+	4	=	47.2	21.1864407
Low to High	Total =	11	+	4.6	+	15	+	4.6	+	12	+	4	=	51.2	19.53125

BREQ, RSTNC, BUSERR

		MPC			BUS LOSS			MPC		Clk skew			
Tristate to Low	Total =	14	+		10	+		15	+	4	=	43	23.255814
Low to Tristate	Total =	12	+		15	+		15	+	4	=	46	21.7391304

LACHn

		MPC		ABT245		BUS LOSS		AS1004		MPC		Clk Skew			
High to Low	Total =	15	+	4.6	+	10	+	4	+	12	+	4	=	49.6	20.1612903
Low to High	Total =	12	+	4.6	+	15	+	4	+	12	+	4	=	51.6	19.379845

ARBITRATION SEQUENCE (over 3-clock cycles)

		MPC Clk-to-data		MPC Logic loop		BUS LOSS		BUS LOSS		MPC Setup		Clk Skew			
	Total =	13 14	+	60	+	20	+	30	+	20	+	4	=	148	20.2702703

TIMING REQUIREMENTS FOR INPUT HOLD TIME

BAD31-BAD0, BPAR3-BPAR0

	MPC Output Hold		ABT245		ABT245		Clk skew		
Output Hold Available =	5	+	1	+	1	-	4	=	3
Input Hold Requirement =	3								

BSC9-BSC0

	MPC Output Hold		ABT245		ABT245		Clk skew		
Output Hold Available =	4	+	1	+	1	-	4	=	2
Input Hold Requirement =	2								

BREQ, RSTNC, BUSERR

	MPC Output Hold		Clk skew		
Output Hold Available =	6.5	-	4	=	2.5
Input Hold Requirement =	0				

ARB5-ARB0

	MPC Output Hold		Clk skew		
Output Hold Available =	6.5	-	4	=	2.5
Input Hold Requirement =	0				

Notes: VOL = 0.55V VOH = 2.0V
Scope probes were attached to the signals on the backplane at the desired slot. Probes were spec'd at 10.8 pF input capacitance.

APPENDIX B

FROM: POLACEK --SIGSCV1 DATE AND TIME 01/30/91 14:44:38
TO: SLSBEA --SIGSCV1 LIEBLERJ--SIGSCV1

SUBJECT: ABT245 DATA FOR INTEL
ATTN: MAGGIE WEAVER
JERRY LIEBLER

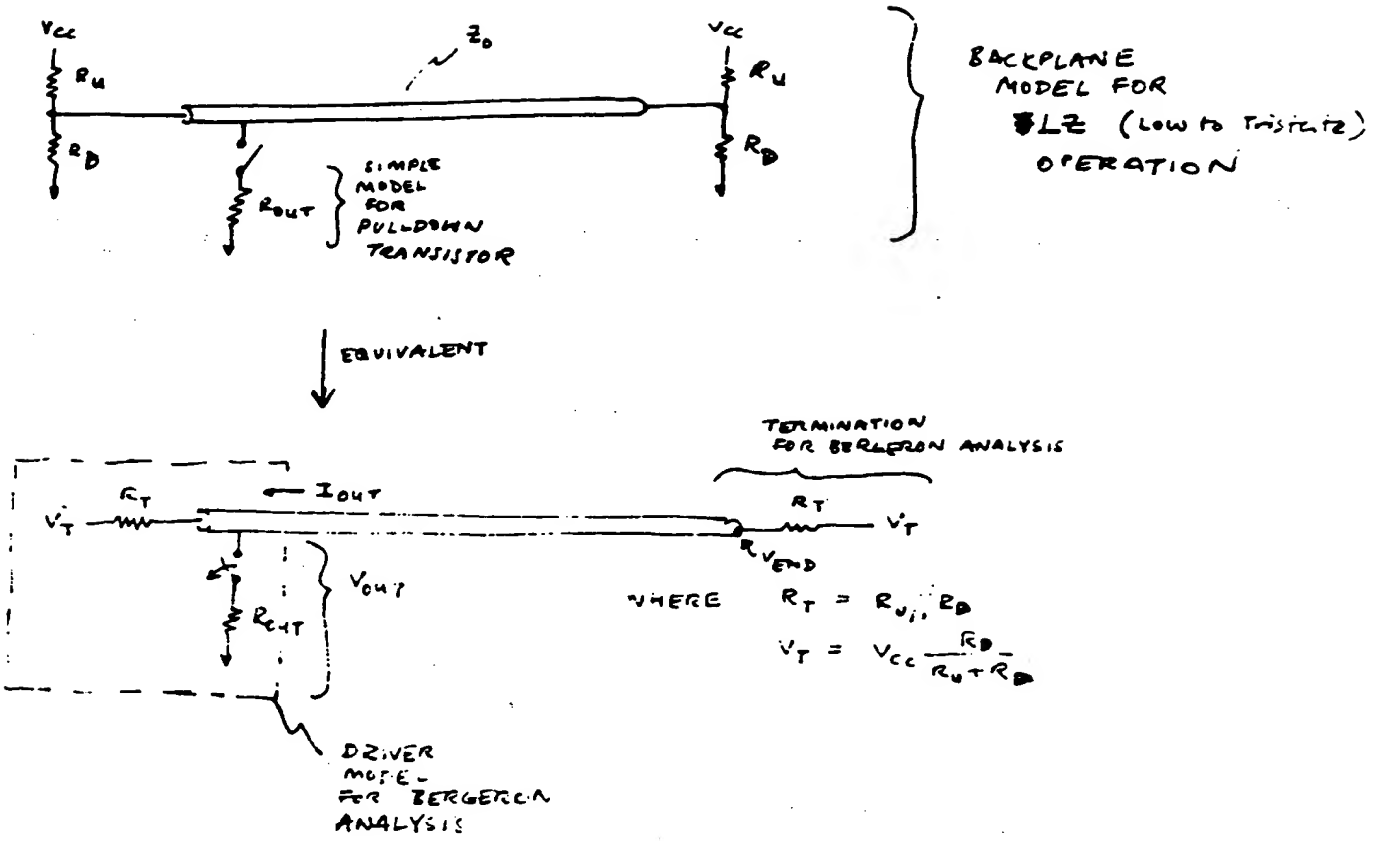
I GOT THE FOLLOWING DATA FROM OREM ON THE ABT244:

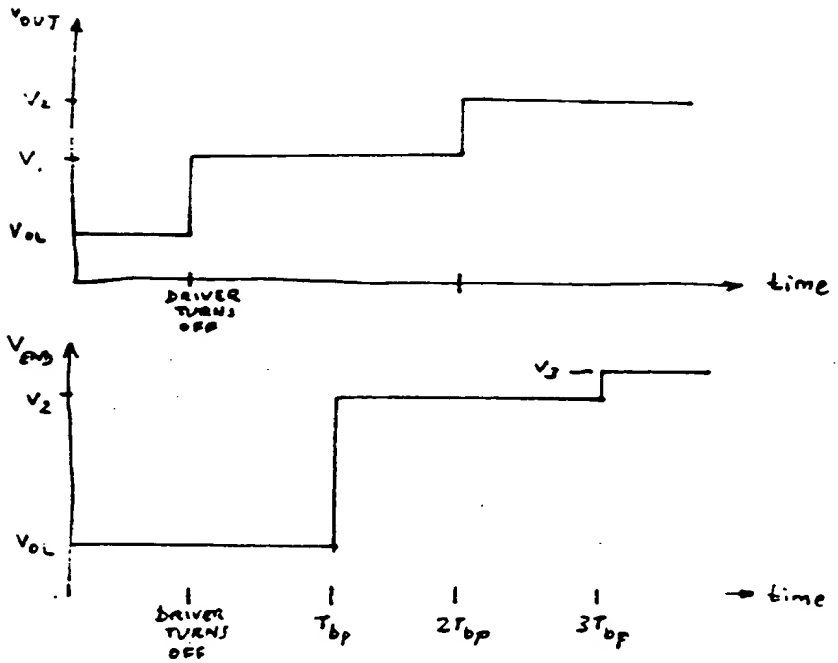
# OF OUTPUTS	PARAMETER	PACKAGE	DELAY
1	TPLH	N	2.6NS
1	TPLH	D	2.3NS
8	TPLH	N	3.3NS (27%)
8	TPLH	D	2.5NS (9%)
1	TPHL	N	2.9NS
1	TPHL	D	2.6NS
8	TPHL	N	4.8NS (66%)
8	TPHL	D	3.3NS (27%)

PLEASE NOTE THE 'N' AND 'D' PARTS WERE FROM DIFFERENT WAFER LOTS THEREFORE THE COMPARISON BETWEEN THEM IS NOT NECESSARILY VALID. THE 1 TO 8 OUTPUT SWITCHING DATA, HOWEVER, IS FROM THE SAME PART.

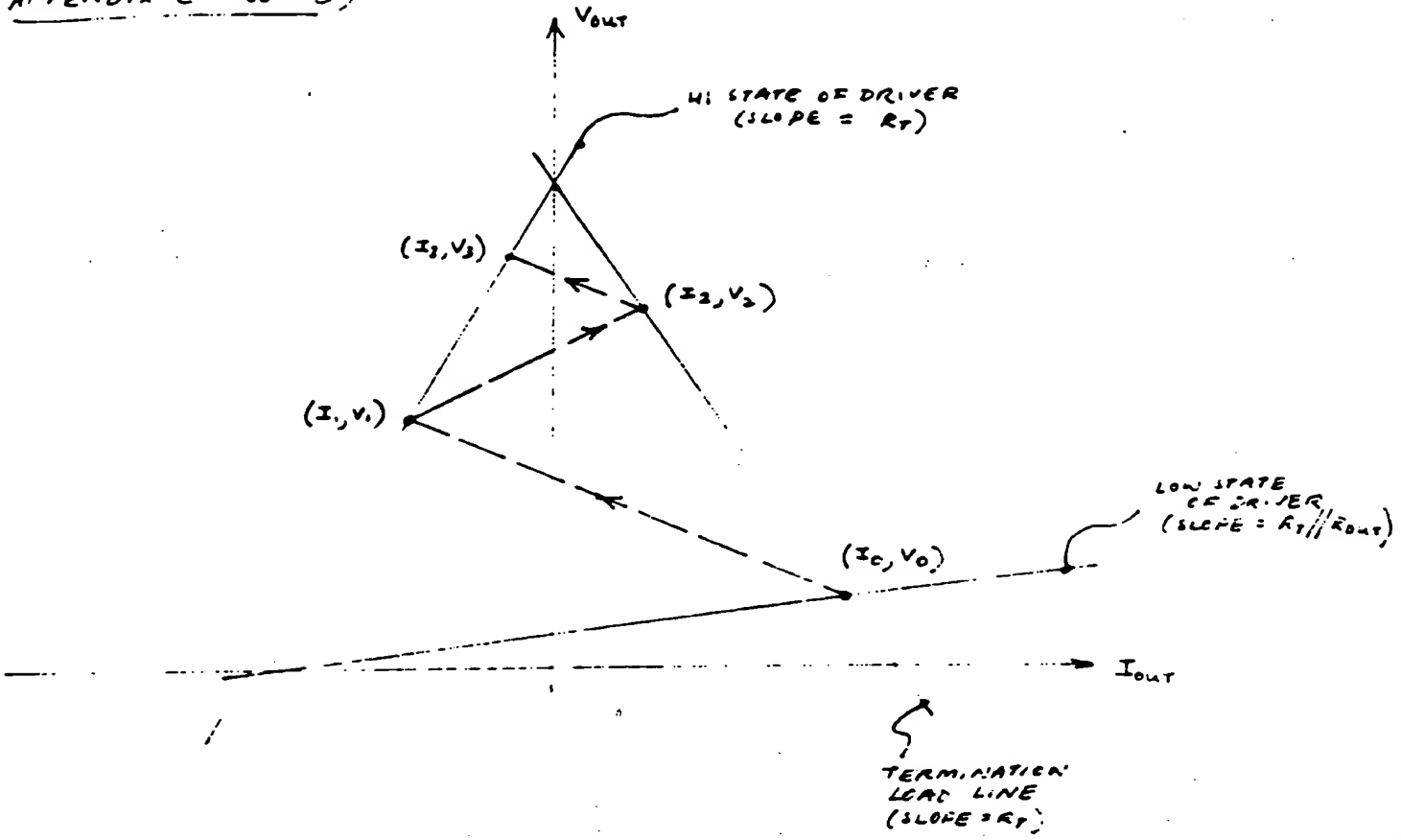
REGARDS,

APPENDIX C


Vcc
RU
RD
Z0
ROUT
SIMPLE MODEL FOR PULLDOWN TRANSISTOR
BACKPLANE MODEL FOR TLZ (LOW to TRISTATE) OPERATION
EQUIVALENT
TERMINATION FOR BERLERON ANALYSIS
RT
VT
IOUT
VOUT
RVEND
WHERE RT = RU, RD
VT = Vcc RD / (RU + RD)
DRIVER MODEL FOR BERGERON ANALYSIS


VOUT
VL
V.
VOL
time
DRIVER TURNS OFF
VEND
V2
V3
VOL
DRIVER TURNS OFF
Tbp
2Tbp
3Tbp
time

APPENDIX C (CONT'D)



AT A LOW STATE $V_O = V_{OL}$ OF DRIVER (0.55V)

THEREFORE $I_{OL} = 2I_O$ (NOT INCLUDING I_{IL}'S OR I_{OZL}'S)

SUBSEQUENTLY,

$$I_0 = \frac{V_T - V_0}{R_T}$$

$$I_1 = \frac{V_T - V_0 + I_0 Z_0}{R_T + Z_0}$$

$$V_1 = V_T - I_1 R_T$$

$$I_2 = \frac{-V_T + V_1 + I_1 Z_0}{R_T + Z_0}$$

$$V_2 = V_T + I_2 Z_0$$

$$I_3 = \frac{V_T - V_2 + I_2 Z_0}{R_T + Z_0}$$

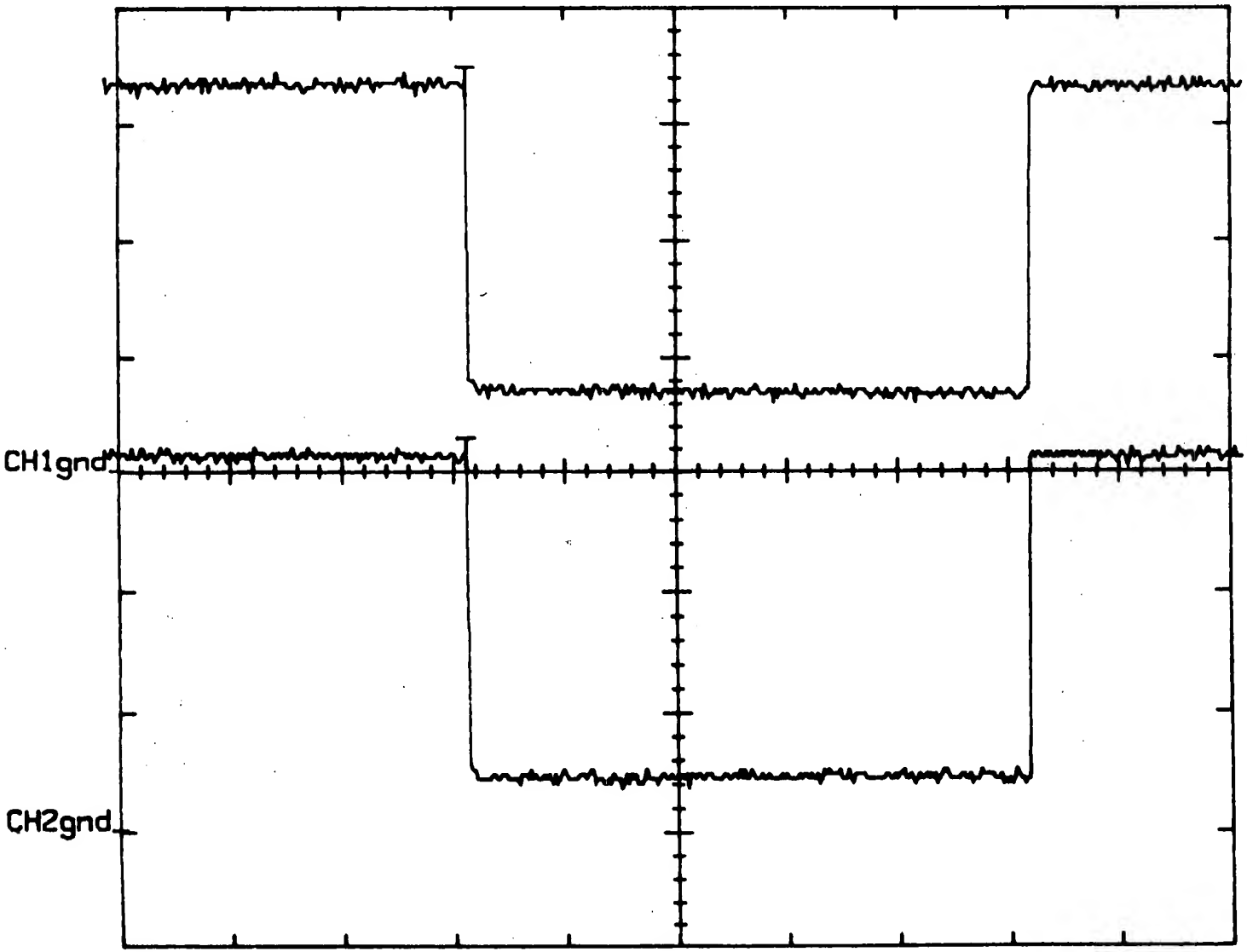
$$V_3 = V_T - I_3 R_T$$

CH1 1V
CH2 1V

Δ 50µs 1.31 V CH2

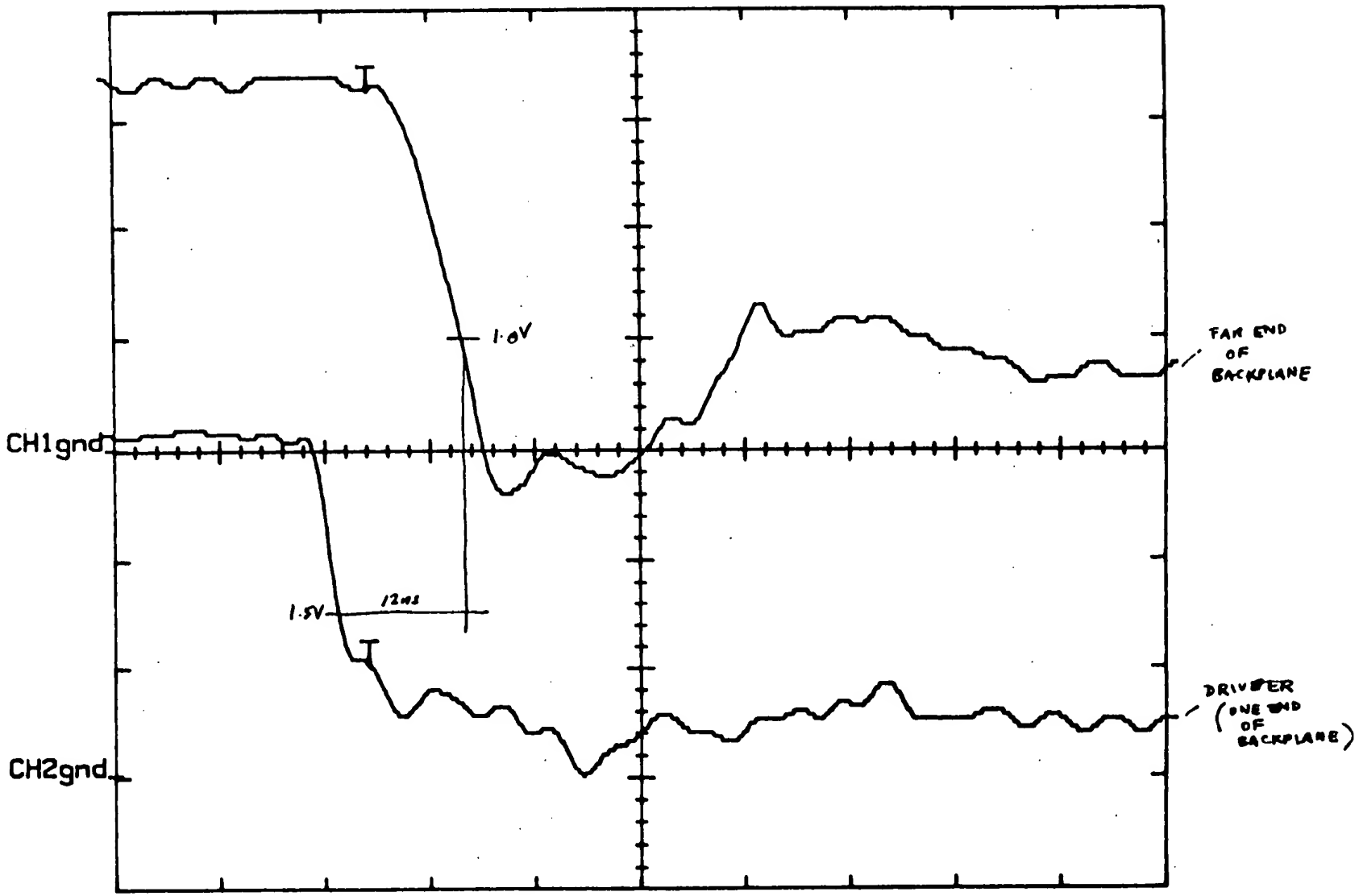
Sc. 2

FR245



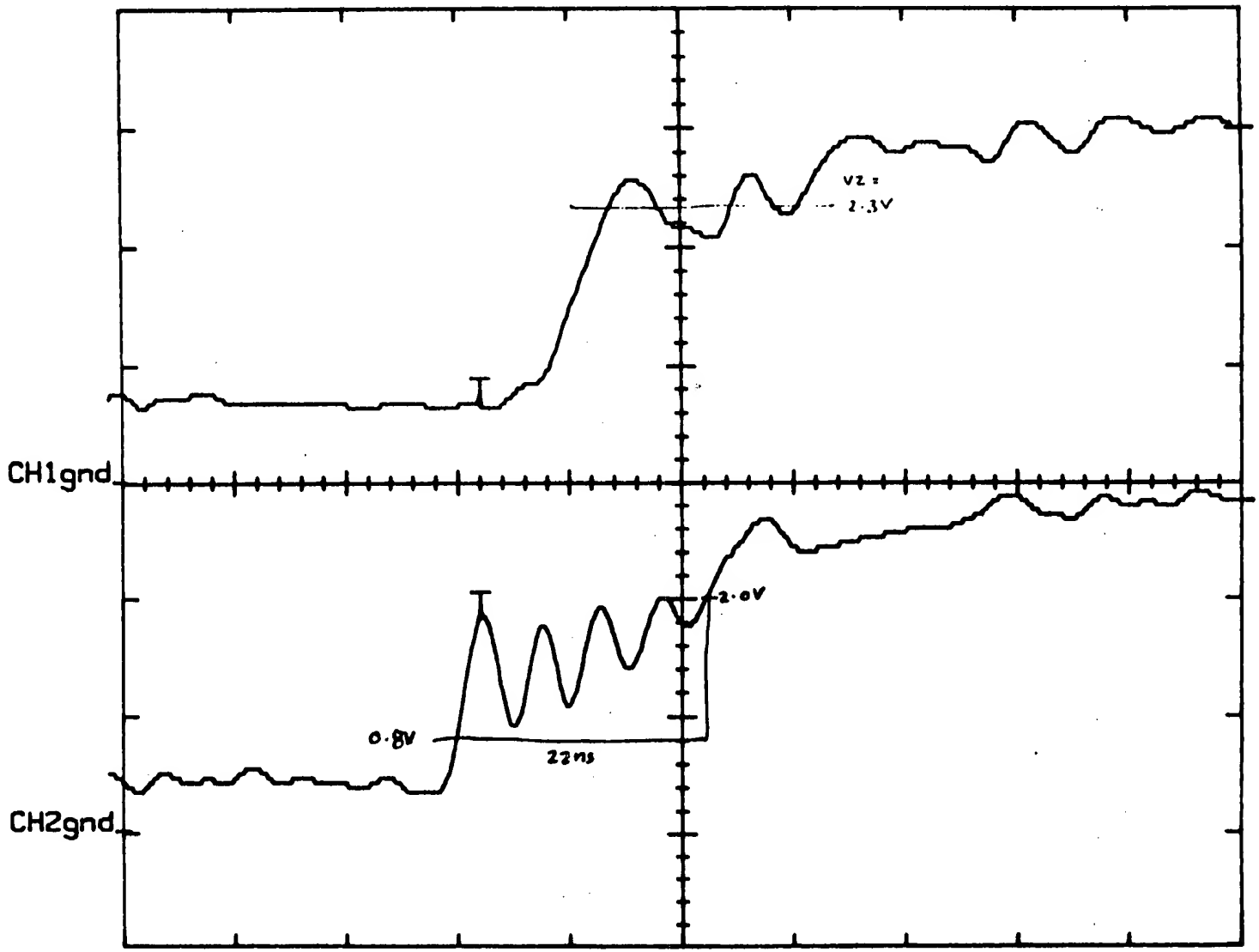
CH1 1V A 10ns 1.31 V CH2
CH2 1V

FR245



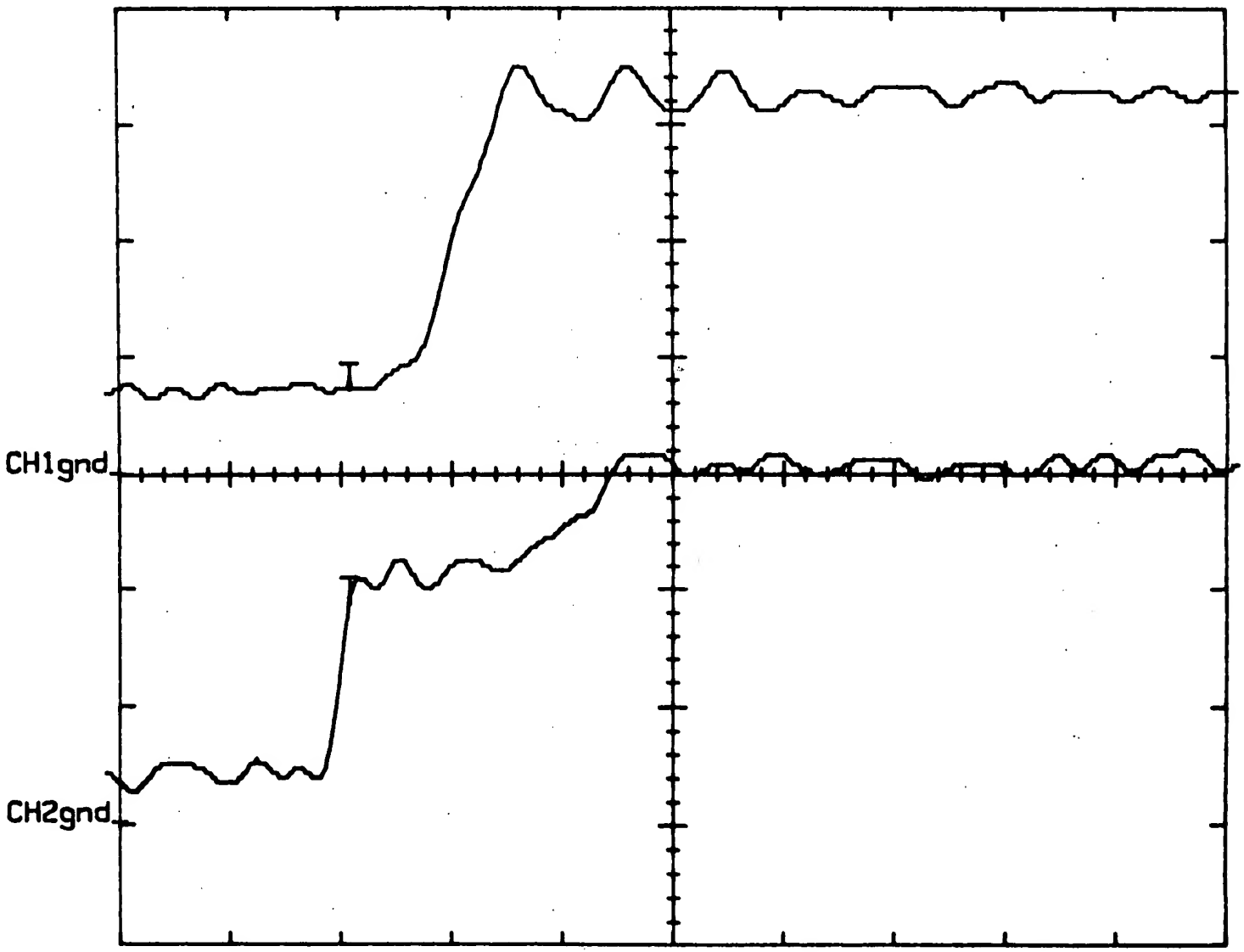
CH1 1V A 10ns 1.31 V CH2
CH2 1V

FR245



CH1 1V A 10ns 1.31 V CH2 L4
CH2 1V

FIR 243

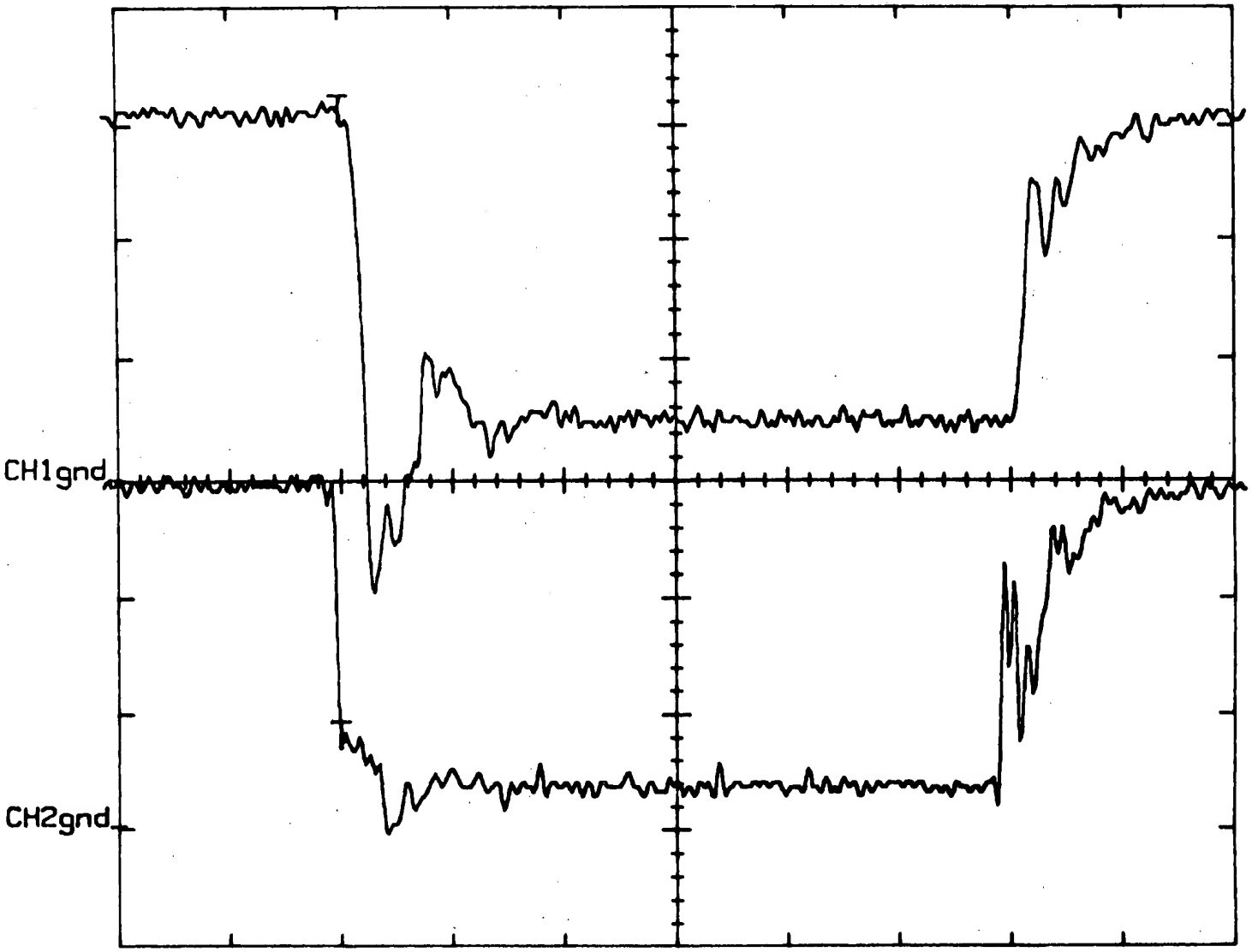


CH1 1V A 50ns 1.31 V CH2

CH2 1V

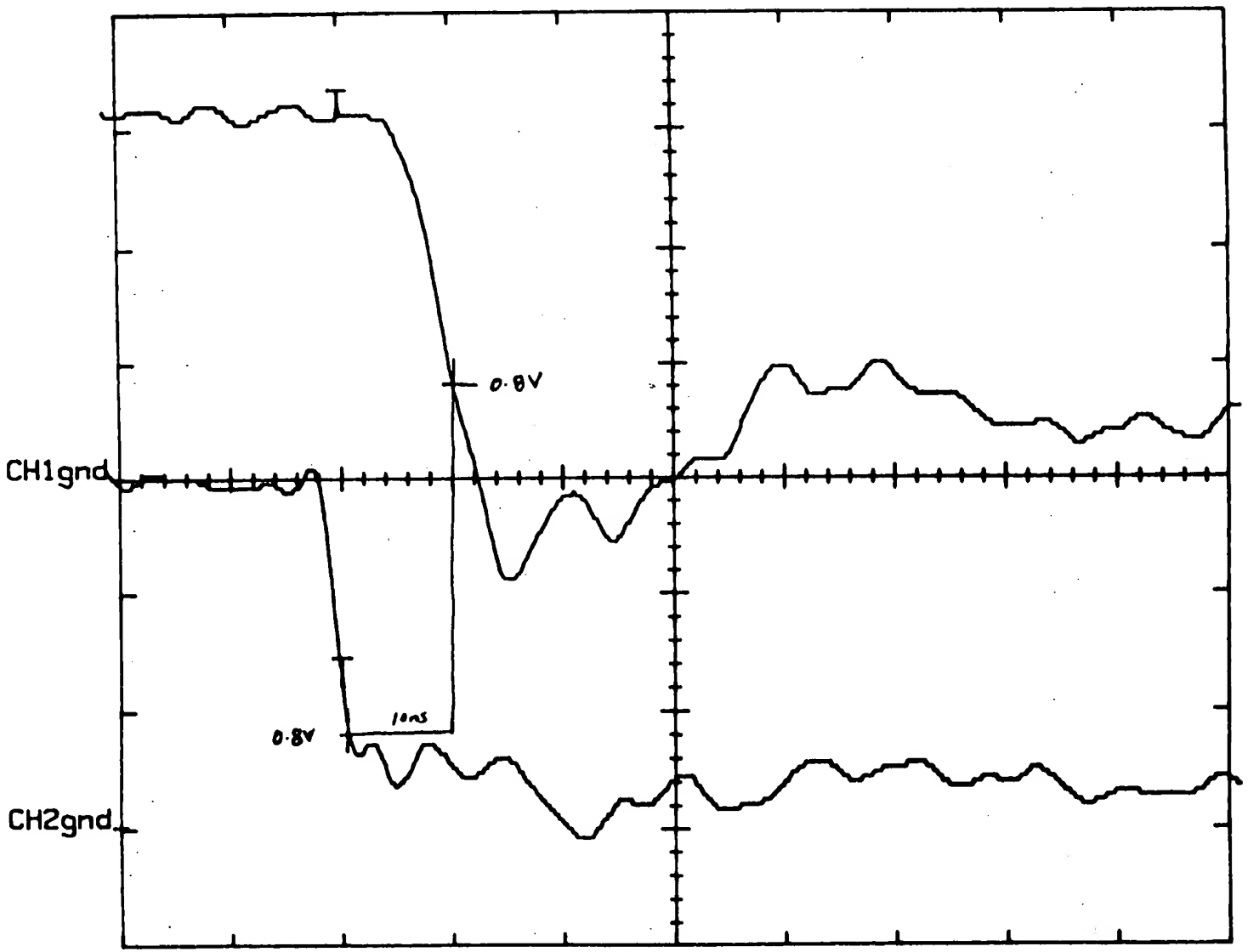
BREQ
Vcc = 4.75V

MPC



CH1 1V A 10ns 1.31 V CH2
CH2 1V

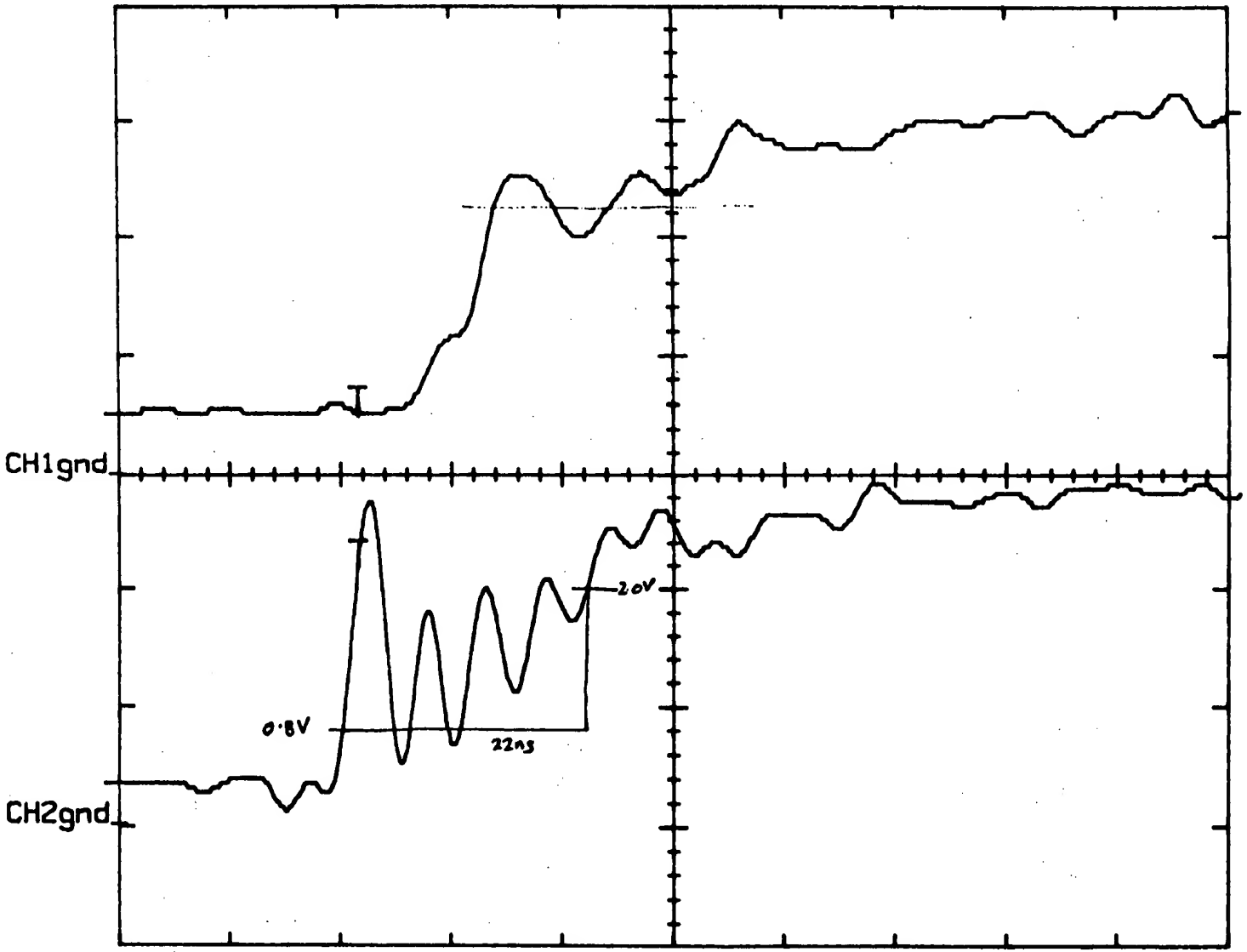
MPC



OREG
Vcc = 4·75V

CH1 1V A 10ns 1.31 V CH2
CH2 1V

MPC



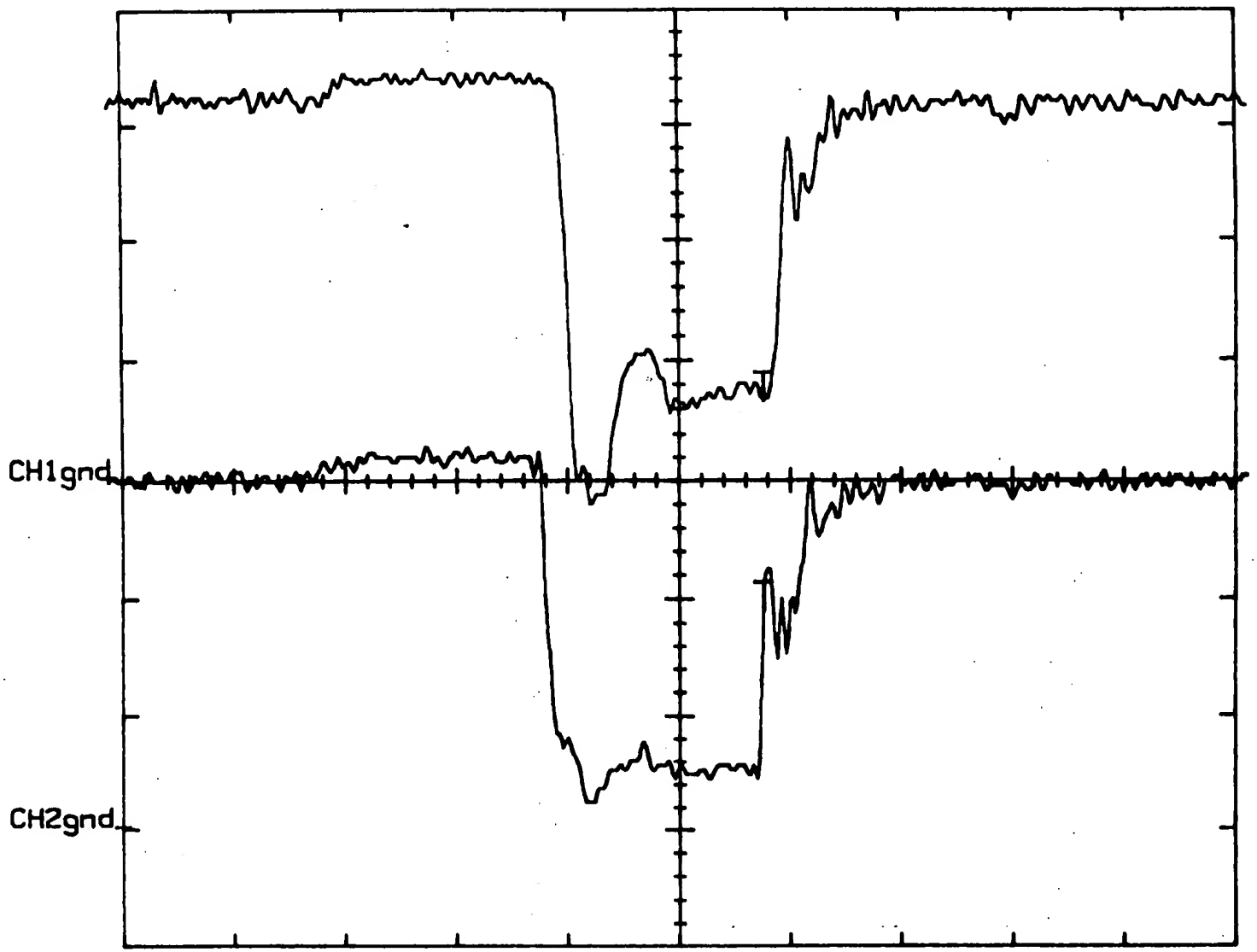
5<4

Vcc : 4.75V

CH1 1V A 50ns 1.31 V CH2

CH2 1V

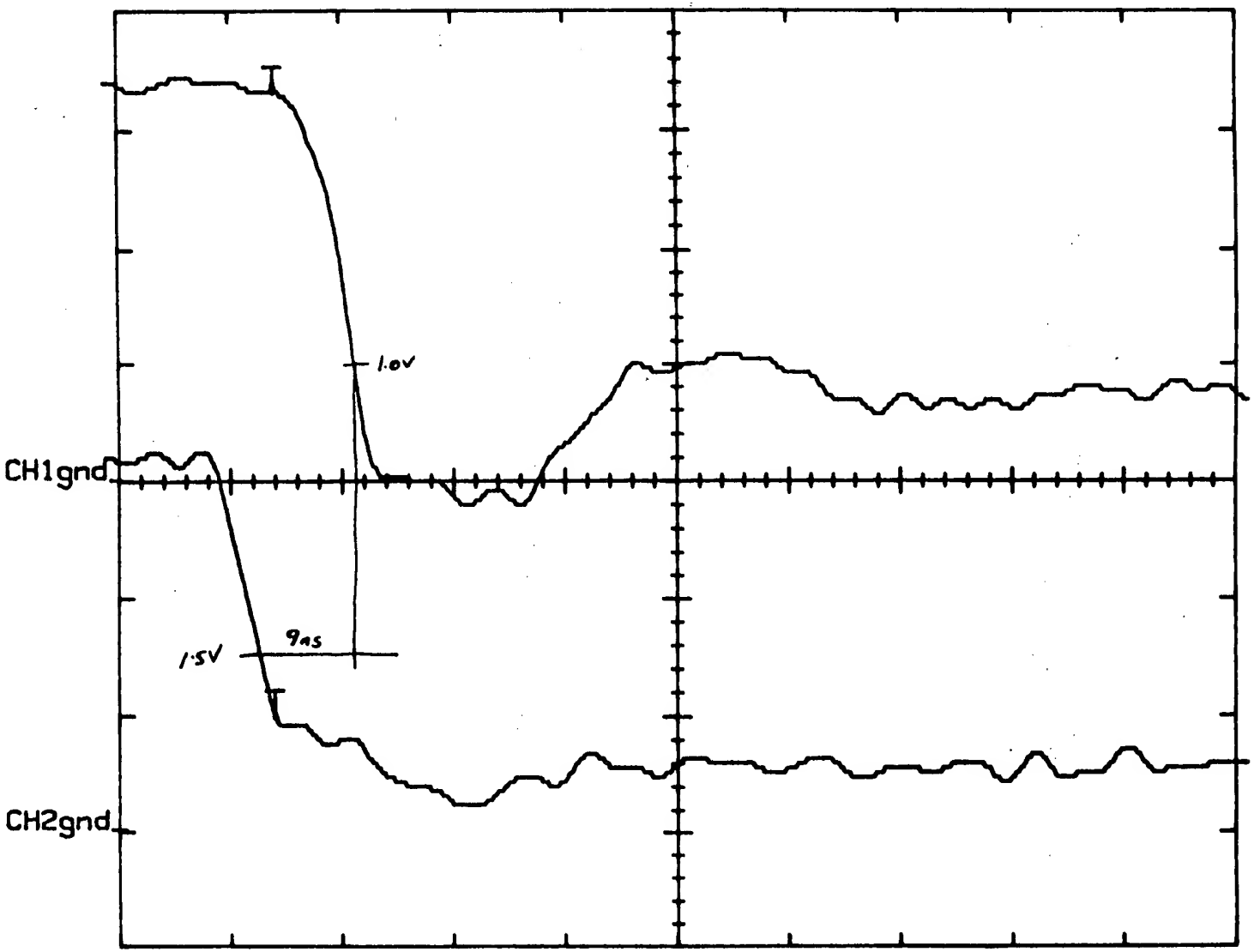
ABT245



5.4
Vcc - 4.75V

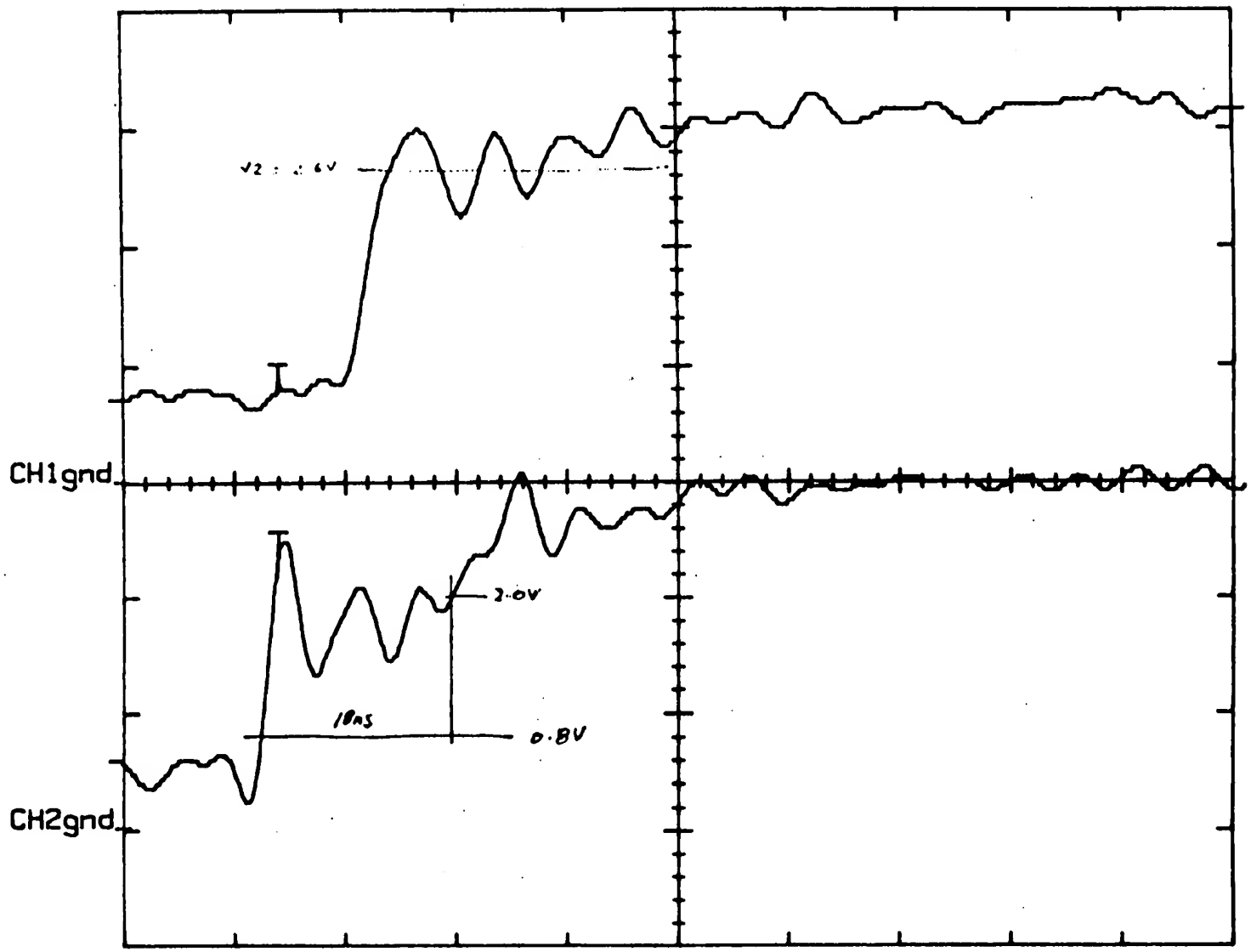
CH1 1V A 10ns 1.31 V CH2
CH2 1V

ABT245



CH1 1V A 10ns 1.31 V CH2
CH2 1V

ABT245



Philips Components—Signetics

Document No.	
ECN No.	853-1447 00227
Date of Issue	August 20, 1990
Status	Product Specification
Advanced BiCMOS Products	

74ABT245

Octal transceiver with direction pin (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT245 device is an octal transceiver featuring noninverting 3-State bus compatible outputs in both send and receive directions. The control function

(continued)

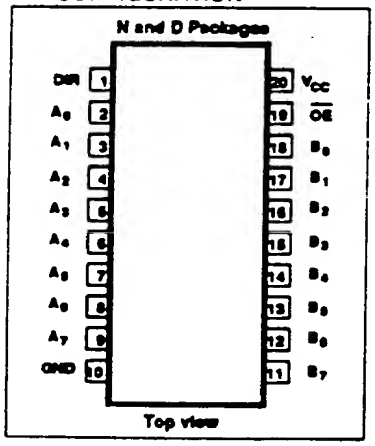
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	2.9	ns
$C_{DIR, \overline{OE}}$	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled: V_{CC} = 5.5V	500	nA

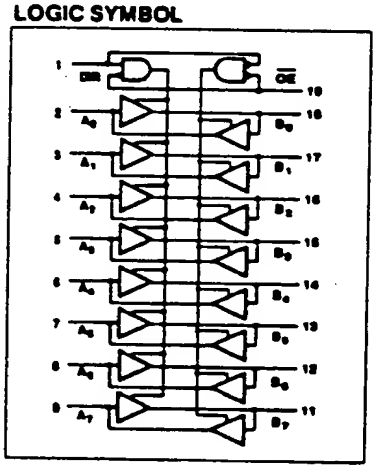
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	-40°C to +85°C	74ABT245N
20-Pin Plastic SOL	-40°C to +85°C	74ABT245D

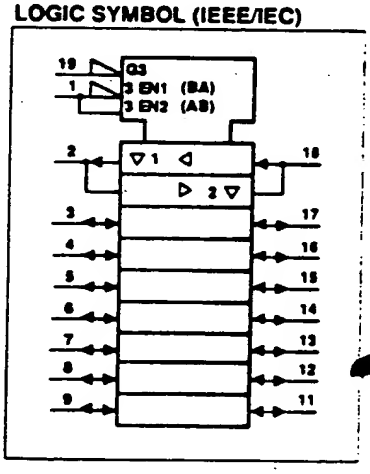
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



tal transceiver with direction pin (3-State)

74ABT245

mentation minimizes external tim- equirements. The device features utput Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

COMMENDED OPERATING CONDITIONS

MBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta V/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

BSOLUTE MAXIMUM RATINGS[1]

YMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

OTES:
Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

JNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A_0 - A_7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B_0 - B_7	Data inputs/outputs (B side)
19	$\overline{OE}$	Ouput enable
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{HI} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{LI} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled; one input at 3.4V; other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State; one data input at 3.4V; other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State; one enable input at 3.4V; other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

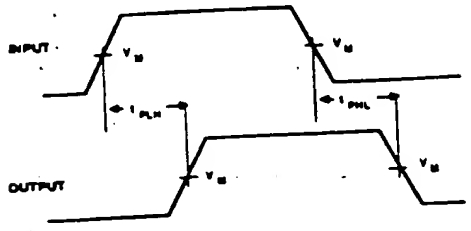
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

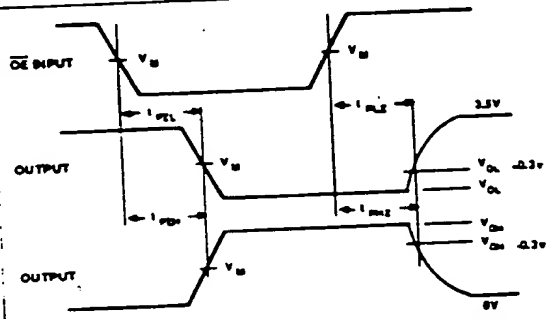
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 2.3	3.3 4.3	4.8 5.8	1.3 2.3	5.3 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.7 2.3	4.7 4.3	6.2 5.8	2.7 2.3	7.2 6.3	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

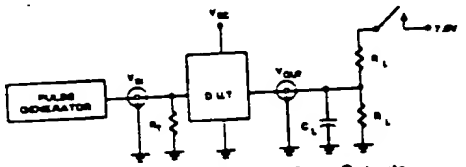


Waveform 1. Waveforms Showing the Input to Output Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

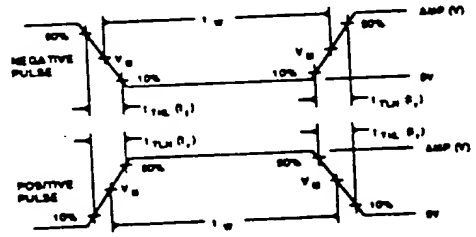
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

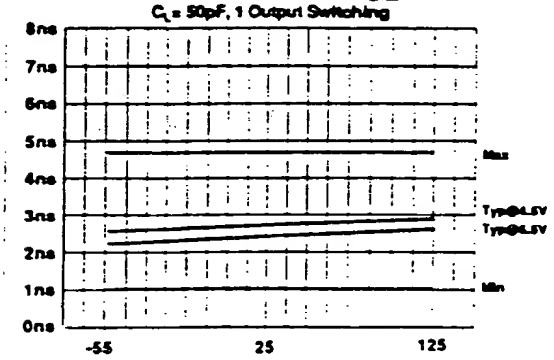


V_M = 1.5V

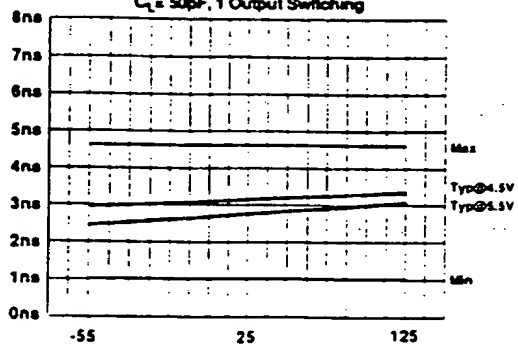
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

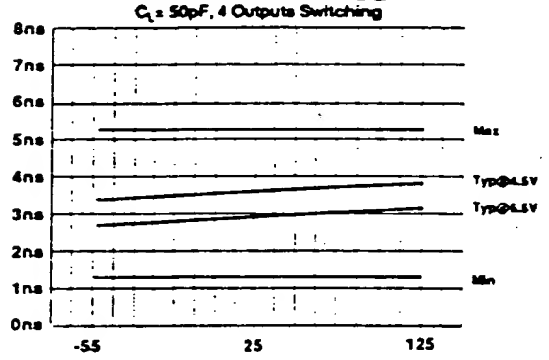
TPLH vs. TEMPERATURE (T_{amb})
C_L = 50pF, 1 Output Switching



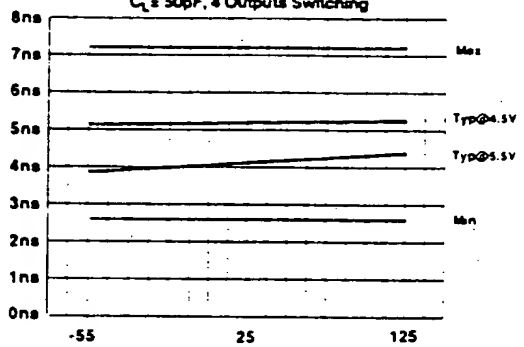
TPHL vs. TEMPERATURE (T_{amb})
C_L = 50pF, 1 Output Switching



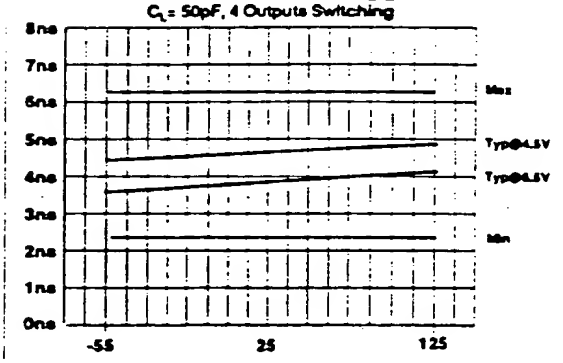
TPZH vs. TEMPERATURE (T_{amb})
C_L = 50pF, 4 Outputs Switching



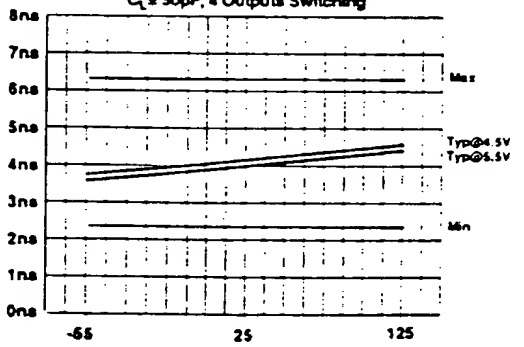
TPHZ vs. TEMPERATURE (T_{amb})
C_L = 50pF, 4 Outputs Switching



TPZL vs. TEMPERATURE (T_{amb})
C_L = 50pF, 4 Outputs Switching



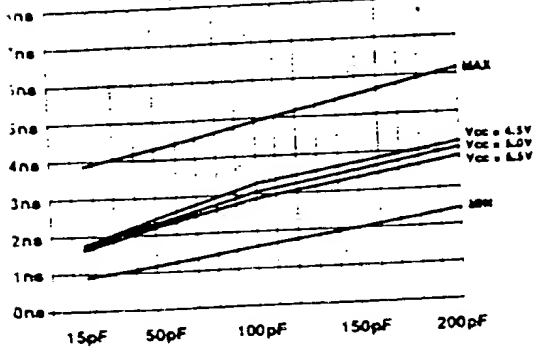
TPLZ vs. TEMPERATURE (T_{amb})
C_L = 50pF, 4 Outputs Switching



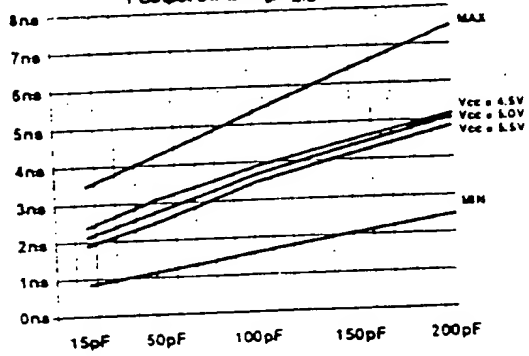
tal transceiver with direction pin (3-State)

74ABT245

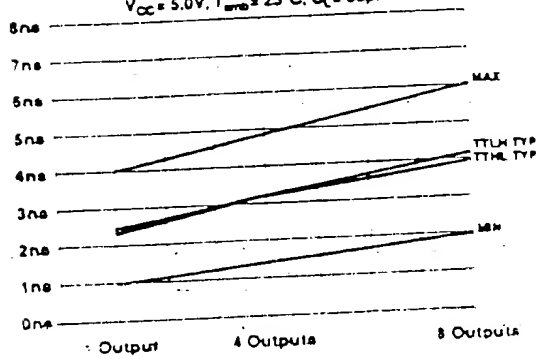
TPLH vs. LOAD CAPACITANCE[1]
1 Output Switching, T_{amb} = 25°C



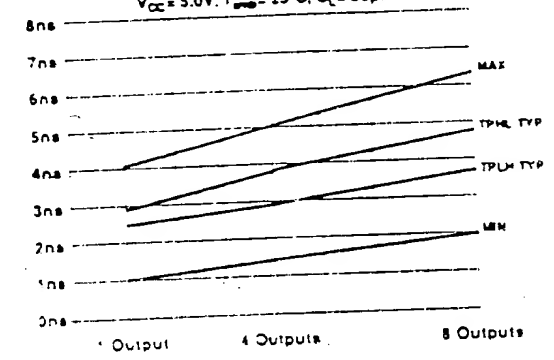
TPHL vs. LOAD CAPACITANCE[1]
1 Output Switching, T_{amb} = 25°C



TTLH TTHL vs. NUMBER OF OUTPUTS SWITCHING[1]
V_{CC} = 5.0V, T_{amb} = 25°C, C_L = 50pF



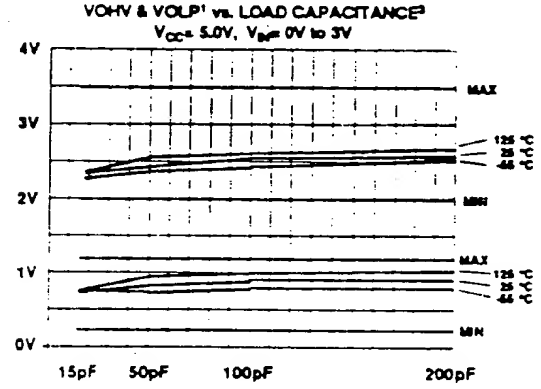
TPLH TPHL vs. NUMBER OF OUTPUTS SWITCHING[1]
V_{CC} = 5.0V, T_{amb} = 25°C, C_L = 50pF

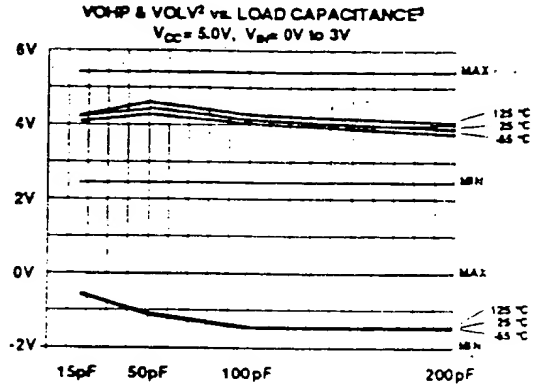


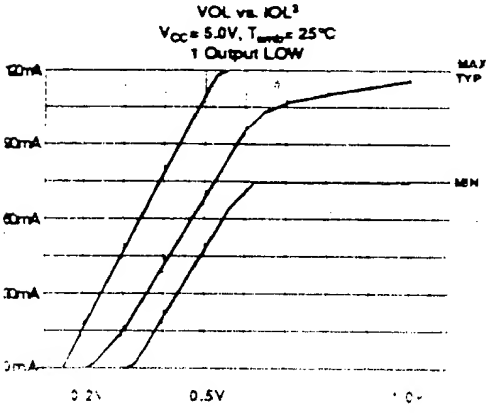
NOTES
MIN and MAX limits are design characteristics and are not necessarily guaranteed values.

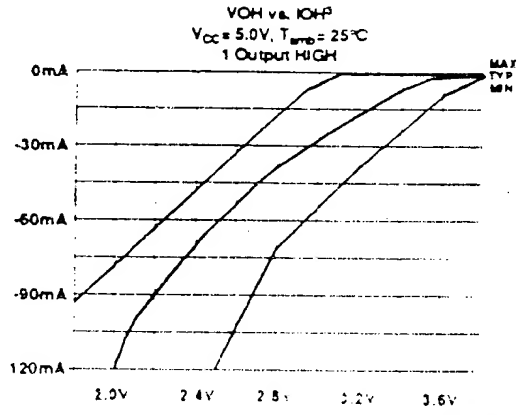
Octal transceiver with direction pin (3-State)

74ABT245









NOTES

1. V_{OHV} is defined as the minimum valley voltage induced on a quiescent high-level output during switching of other outputs. V_{OLP} is defined as the maximum peak voltage induced on a quiescent low-level output during switching of other outputs.
2. V_{OHP} is defined as the maximum peak voltage induced on a quiescent high-level output during switching of other outputs. V_{OLV} is defined as the minimum valley voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX limits are design and process characteristics. They are not tested but guaranteed by the

FEATURES

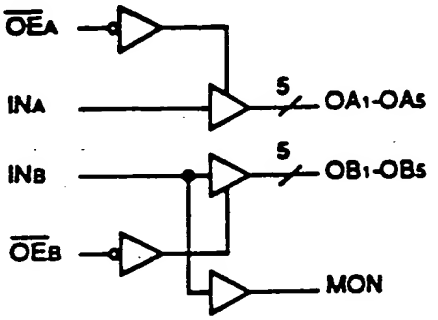
Equivalent to FAST™ output drive over full temperature and voltage supply extremes
I_{OL} = 64mA (commercial) and 48mA (military)
CMOS power levels (1mW typ. static)
TTL input and output level compatible
CMOS output level compatible
Two independent groups of buffers with 3-state control
5:1 fanout (1 in - 5 out) per group
True and inverting options
'Heartbeat' monitor output
Guaranteed low skew
Pinout designed for minimum skew and ground bounce
Clock busing with 3-state control
20 pin DIP, SOIC, CERPACK and LCC
Meets or exceeds JEDEC Standard 18 specifications
Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT49FCT805/A and IDT49FCT806/A are clock drivers built using advanced CEMOS™, a dual metal CMOS technology. The IDT49FCT805A is a non-inverting clock driver and the IDT49FCT806A is an inverting clock driver. Each clock driver consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible CMOS input.

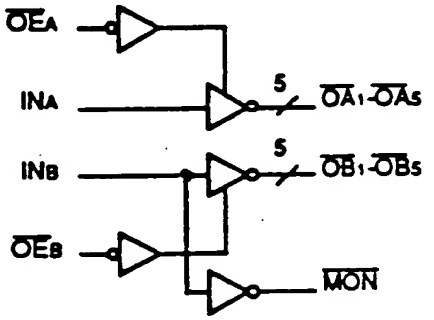
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805



2574 drw 03

IDT49FCT806

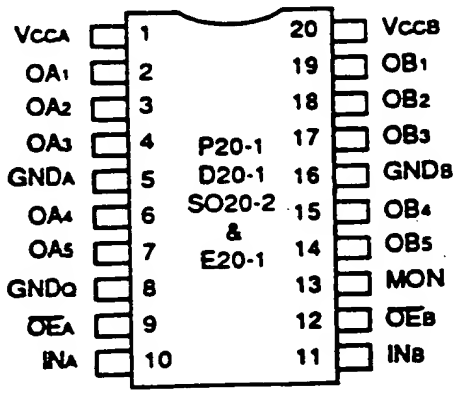


2574 drw 08

FAST is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

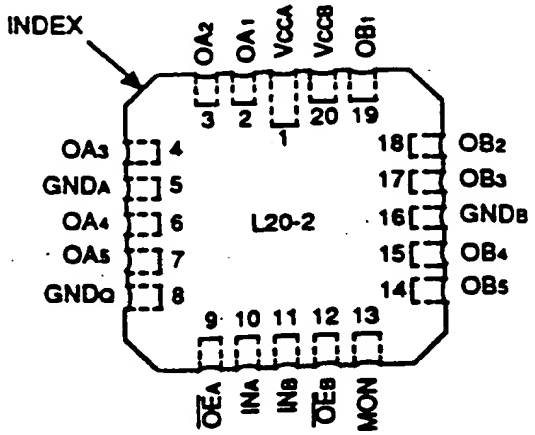
PIN CONFIGURATIONS

49FCT805



DIP/SOIC/CERPACK
TOP VIEW

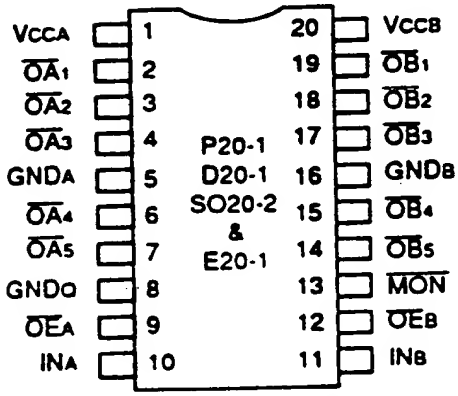
2574 drw 01



LCC
TOP VIEW

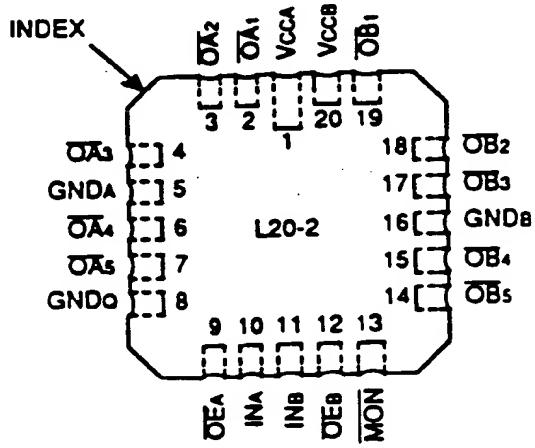
2574 drw 02

IDT49FCT806



DIP/SOIC/CERPACK
TOP VIEW

2574 drw 04



LCC
TOP VIEW

2574 drw 05

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OAn, OBn	Clock Outputs
MON	Monitor Output

2574 tbl 05

FUNCTION TABLE[1]

Inputs		Outputs			
		49FCT805		49FCT806	
$\overline{OE}_A$, $\overline{OE}_B$	INA, INB	OAn, OBn	MON	$\overline{OA}_n$, $\overline{OB}_n$	$\overline{MON}$
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

2574 tbl 06

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2574 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
   Input and Vcc terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2574 tbl 0

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: TA = 0°C to +70°C; VCC = 5.0V ± 5%, Military: TA = −55°C to +125°C; VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = GND	—	—	−5	µA
I_{OZH}	Off State (HIGH Z) Output Current	Vcc = Max.	V_O = Vcc	—	—	10	µA
I_{OZL}			V_O = GND	—	—	−10	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		−60	−120	−225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	3.6	4.3	—	V
			I_{OH} = −24mA MIL. I_{OH} = −24mA COM'L.	2.4	3.8	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis for all inputs	Vcc = 5V		—	200	—	mV

NOTES: 2574 tbl 00

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

WER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND Per Output Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Five Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	7.7	14.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	8.0	15.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	4.3	8.4[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.8	10.4[5]	

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ES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition (1)	IDT49FCT805/806				IDT49FCT805A/806A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. (2)	Max.	Min. (2)	Max.	Min. (2)	Max.	Min. (2)	Max.	
t_{PLH} t_{PHL}	Propagation Delay I_{NA} to O_{An}, I_{NB} to O_{Bn}	C_L = 50pF R_L = 500Ω	1.5	6.5			1.5	5.8			ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to O_{An}, $\overline{OE}_B$ to O_{Bn}		1.5	8.0			1.5	8.0			ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to O_{An}, $\overline{OE}_B$ to O_{Bn}		1.5	7.0			1.5	7.0			ns
$t_{SK(o)}$ (3)	Skew between two outputs of same package (same transition)		—	0.7			—	0.7			ns
$T_{SK(p)}$ (3)	Skew between opposite transitions (t_{PHL} - t_{PLH}) of same output		—	1.0			—	1.0			ns
$T_{SK(t)}$ (3)	Skew between two outputs of different package at same power supply voltage and temperature (same transition)		—	1.5			—	1.5			ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew guaranteed across temperature range but measured at maximum temperature only. Skew parameters apply to propagation delays only.

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